Annex L: Serial Presence Detect (SPD) for DDR4 SDRAM Modules

DDR4 SPD Document Release 2

UDIMM Revision 1.0

RDIMM Revision 1.0

LRDIMM Revision 1.0

1.0 Introduction

This annex describes the serial presence detect (SPD) values for all DDR4 modules. Differences between module types are encapsulated in subsections of this annex. These presence detect values are those referenced in the SPD standard document for 'Specific Features'. The following SPD fields will be documented in the order presented in section 1.1 with the exception of bytes 128~255 which are documented in separate annexes, one for each family of module types. Further description of Byte 2 is found in Annex A of the SPD standard.

All unused entries will be coded as 0x00. All unused bits in defined bytes will be coded as 0 except where noted.

DDR4 generation systems are required to check the voltages supported by the DRAMs by reading the SPD and parsing byte 6, the Module Nominal Voltage, before applying power to the DRAMs. All JEDEC standard modules allow applying SPD power without applying a supply voltage to the DRAMs in order to support this requirement.

Timing parameters in the SPD represent the operation of the module including all DRAMs and support devices at the lowest supported supply voltage (see SPD byte 11), and are valid from t_{CKAVG}min to t_{CKAVG}max (see SPD bytes 18 and 19).

To allow for maximum flexibility as devices evolve, SPD fields described in this document may support device configuration and timing options that are not included in the JEDEC DDR4 SDRAM data sheet (JESD79-4). Please refer to DRAM supplier data sheets or JESD79-4 to determine the compatibility of components.

1.1 Address map

The following is the SPD address map for all DDR4 modules. It describes where the individual lookup table entries will be held in the serial EEPROM. Consistent with the definition of DDR4 generation SPD devices, which have four individual write protection blocks of 128 bytes in length each, the SPD contents are aligned with these blocks as follows:

Block	Range		Description
0	0~127	0x000~0x07F	Base Configuration and DRAM Parameters
1	128~255	0x080~0x0FF	Module Specific Parameters -- See subsections L1, L2, and L3 for details
2	256~319	0x100~0x13F	Reserved -- must be coded as 0x00
	320~383	0x140~0x17F	Manufacturing Information
3	384~511	0x180~0x1FF	End User Programmable

Block 0: Base Configuration and DRAM Parameters

The following table details the location of each byte in this block.

Byte Number		Function Described	Notes
0	0x000	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	1, 2
1	0x001	SPD Revision	
2	0x002	Key Byte / DRAM Device Type	
3	0x003	Key Byte / Module Type	
4	0x004	SDRAM Density and Banks	3
5	0x005	SDRAM Addressing	3
6	0x006	SDRAM Package Type	3
7	0x007	SDRAM Optional Features	3
8	0x008	SDRAM Thermal and Refresh Options	3
9	0x009	Other SDRAM Optional Features	3
10	0x00A	Reserved -- must be coded as 0x00	
11	0x00B	Module Nominal Voltage, VDD	3
12	0x00C	Module Organization	
13	0x00D	Module Memory Bus Width	
14	0x00E	Module Thermal Sensor	
15	0x00F	Extended module type	
16	0x010	Reserved -- must be coded as 0x00	
17	0x011	Timebases	
18	0x012	SDRAM Minimum Cycle Time (t_{CKAVG}min)	3
19	0x013	SDRAM Maximum Cycle Time (t_{CKAVG}max)	3
20	0x014	CAS Latencies Supported, First Byte	3
21	0x015	CAS Latencies Supported, Second Byte	3
22	0x016	CAS Latencies Supported, Third Byte	3
23	0x017	CAS Latencies Supported, Fourth Byte	3
24	0x018	Minimum CAS Latency Time (t_{AA}min)	3

Note 1 Number of SPD bytes written will typically be programmed as 384 bytes.
Note 2 Size of SPD device will typically be programmed as 512 bytes.
Note 3 From DDR4 SDRAM datasheet.
Note 4 These are optional, in accordance with the JEDEC specification.

Byte Number		Function Described	Notes
25	0x019	Minimum RAS to CAS Delay Time (t_{RCD}min)	3
26	0x01A	Minimum Row Precharge Delay Time (t_{RP}min)	3
27	0x01B	Upper Nibbles for t_{RAS}min and t_{RC}min	3
28	0x01C	Minimum Active to Precharge Delay Time (t_{RAS}min), Least Significant Byte	3
29	0x01D	Minimum Active to Active/Refresh Delay Time (t_{RC}min), Least Significant Byte	3
30	0x01E	Minimum Refresh Recovery Delay Time (t_{RFC1}min), LSB	3
31	0x01F	Minimum Refresh Recovery Delay Time (t_{RFC1}min), MSB	3
32	0x020	Minimum Refresh Recovery Delay Time (t_{RFC2}min), LSB	3
33	0x021	Minimum Refresh Recovery Delay Time (t_{RFC2}min), MSB	3
34	0x022	Minimum Refresh Recovery Delay Time (t_{RFC4}min), LSB	3
35	0x023	Minimum Refresh Recovery Delay Time (t_{RFC4}min), MSB	3
36	0x024	Minimum Four Activate Window Time (t_{FAW}min), Most Significant Nibble	3
37	0x025	Minimum Four Activate Window Time (t_{FAW}min), Least Significant Byte	3
38	0x026	Minimum Activate to Activate Delay Time (t_{RRD_S}min), different bank group	3
39	0x027	Minimum Activate to Activate Delay Time (t_{RRD_L}min), same bank group	3
40	0x28	Minimum CAS to CAS Delay Time (t_{CCD_L}min), same bank group	3
41~59	0x029~0x03B	Reserved -- must be coded as 0x00	
60~77	0x03C~0x04D	Connector to SDRAM Bit Mapping	
78~116	0x04E~0x074	Reserved -- must be coded as 0x00	
117	0x75	Fine Offset for Minimum CAS to CAS Delay Time (t_{CCD_L}min), same bank group	
118	0x76	Fine Offset for Minimum Activate to Activate Delay Time (t_{RRD_L}min), same bank group	3
119	0x77	Fine Offset for Minimum Activate to Activate Delay Time (t_{RRD_S}min), different bank group	3
120	0x078	Fine Offset for Minimum Activate to Activate/Refresh Delay Time (t_{RC}min)	3
121	0x079	Fine Offset for Minimum Row Precharge Delay Time (t_{RP}min)	3
122	0x07A	Fine Offset for Minimum RAS to CAS Delay Time (t_{RCD}min)	3
123	0x07B	Fine Offset for Minimum CAS Latency Time (t_{AA}min)	3
124	0x07C	Fine Offset for SDRAM Maximum Cycle Time (t_{CKAVG}max)	3
125	0x07D	Fine Offset for SDRAM Minimum Cycle Time (t_{CKAVG}min)	3
126	0x07E	CRC for Base Configuration Section, Least Significant Byte	
127	0x07F	CRC for Base Configuration Section, Most Significant Byte	

Note 1 Number of SPD bytes written will typically be programmed as 384 bytes.
Note 2 Size of SPD device will typically be programmed as 512 bytes.
Note 3 From DDR4 SDRAM datasheet.
Note 4 These are optional, in accordance with the JEDEC specification.

Block 1: Module Specific Parameters

Bytes 128~255 (0x080~0x0FF) Parameters in this block are specific to the module type as selected by the contents of SPD Key Byte 3. Refer to the appropriate annex for detailed byte descriptions.

Block 2, lower half: Reserved

Bytes 256~319 (0x100~0x13F) Reserved -- must be coded as 0x00.

Block 2, upper half: Manufacturing Information

Bytes 320~383 (0x140~0x17F) The following table details the location of each byte in this block.

Byte Number		Function Described	Notes
320	0x140	Module Manufacturer's ID Code, Least Significant Byte	
321	0x141	Module Manufacturer's ID Code, Most Significant Byte	
322	0x142	Module Manufacturing Location	
323~324	0x143~0x144	Module Manufacturing Date	
325~328	0x145~0x148	Module Serial Number	
329~348	0x149~0x15C	Module Part Number	
349	0x15D	Module Revision Code	
350	0x15E	DRAM Manufacturer's ID Code, Least Significant Byte	
351	0x15F	DRAM Manufacturer's ID Code, Most Significant Byte	
352	0x160	DRAM Stepping	
353~381	0x161~0x17D	Module Manufacturer's Specific Data	
382~383	0x17E~0x17F	Reserved; must be coded as 0x00	

Block 3: End User Programmable

Bytes 384~511 (0x180~0x1FF) Bytes in this block are reserved for use by end users.

2.0 Details of each byte

2.1 General Configuration Section: Bytes 0~127 (0x000~0x07F)

This section contains defines parameters that are common to all DDR4 module types.

Byte 0 (0x000): Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage

The least significant nibble of this byte describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data. Bits 6~4 describe the total size of the serial memory used to hold the Serial Presence Detect data.

Bit 7	Bits 6~4	Bits 3~0
Reserved	**SPD Bytes Total**	**SPD Bytes Used**
Reserved	Bit [6, 5, 4] : 000 = Undefined 001 = 256 010 = 512 All others reserved	Bit [3, 2, 1, 0] : 0000 = Undefined 0001 = 128 0010 = 256 0011 = 384 0100 = 512 All others reserved
Note 1 Typical programming of bits 3~0 will be 0011 (384 bytes).		

Byte 1 (0x001): SPD Revision

This byte describes the compatibility level of the encoding of the bytes contained in the SPD EEPROM, and the current collection of valid defined bytes. Software should examine the upper nibble (Encoding Level) to determine if it can correctly interpret the contents of the module SPD. The lower nibble (Additions Level) can optionally be used to determine which additional bytes or attribute bits have been defined; however, since any undefined additional byte must be encoded as 0x00 or undefined attribute bit must be defined as 0, software can safely detect additional bytes and use safe defaults if a zero encoding is read for these bytes.

Production Status	SPD Revision	Encoding Level				Additions Level				Hex
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Pre-production	Revision 0.0	0	0	0	0	0	0	0	0	00
	Revision 0.1	0	0	0	0	0	0	0	1	01
	...	.	.	.	.	.	.	.	.	.
	Revision 0.9	0	0	0	0	1	0	0	1	09
Production	Revision 1.0	0	0	0	1	0	0	0	0	10
	Revision 1.1	0	0	0	1	0	0	0	1	11
	...	.	.	.	.	.	.	.	.	...
Undefined	Undefined	1	1	1	1	1	1	1	1	FF

The Additions Level is never reduced even after an increment of the Encoding Level. For example, if the current SPD revision level were 1.2 and a change in Encoding Level were approved, the next revision level would be 2.2. If additions to revision 2.2 were approved, the next revision would be 2.3. Changes in the Encoding Level are extremely rare, however, since they can create incompatibilities with older systems.

The exceptions to the above rule are the SPD revision levels used during development prior to the Revision 1.0 release. Revisions 0.0 through 0.9 are used to indicate sequential pre-production SPD revision levels, however the first production release will be Revision 1.0.

This document defines the SPD contents for multiple families of DDR4 memory modules, with a separate subsection of this Annex for each family that defines the bytes in SPD locations 128~255 (0x080~0x0FF). These module families and their respective subsections are:

- Annex L.1: Unbuffered Memory Modules
- Annex L.2: Registered Memory Modules
- Annex L.3: Load Reduced Memory Modules

The SPD revision level for each module family type is independent. This allows changes to be made to the Registered DIMM annex, for example, without necessarily changing the revision of Unbuffered DIMMs. In this context, the SPD revision value corresponds to all SPD bytes *for that DIMM type*. It also means that over time, the revisions for each module type may vary. Note that changes to a DIMM specific annex do not affect the revisions of other module types, but changes in the General Section of the SPD affect all DIMM types. The following example suggests a possible historical progression:

Table 1 — Hypothetical Historic Progression of SPD Revisions by DIMM Type

Event	UDIMM	RDIMM	LRDIMM
Initial SPD release	1.0	1.0	1.0
Addition in RDIMM Annex	1.0	1.1	1.0
Addition in LRDIMM Annex	1.0	1.1	1.1
Addition in LRDIMM Annex	1.0	1.1	1.2
Addition in General Section	1.1	1.2	1.3
Addition in UDIMM Annex	1.2	1.2	1.3
Encoding change in LRDIMM Annex	1.2	1.2	2.3
Addition in LRDIMM Annex	1.2	1.2	2.4
Encoding change in General Section	2.2	2.2	3.4
Addition in RDIMM Annex	2.2	2.3	3.4

Byte 2 (0x002): Key Byte / DRAM Device Type

This byte is the key byte used by the system BIOS to determine how to interpret all other bytes in the SPD EEPROM. The BIOS must check this byte first to ensure that the EEPROM data is interpreted correctly. Any DRAM or Module type that requires significant changes to the SPD format (beyond defining previously undefined bytes or bits) also requires a new entry in the key byte table below.

Line #	SDRAM / Module Type Corresponding to Key Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Reserved	0	0	0	0	0	0	0	0	00
1	Fast Page Mode	0	0	0	0	0	0	0	1	01
2	EDO	0	0	0	0	0	0	1	0	02
3	Pipelined Nibble	0	0	0	0	0	0	1	1	03
4	SDRAM	0	0	0	0	0	1	0	0	04
5	ROM	0	0	0	0	0	1	0	1	05
6	DDR SGRAM	0	0	0	0	0	1	1	0	06
7	DDR SDRAM	0	0	0	0	0	1	1	1	07
8	DDR2 SDRAM	0	0	0	0	1	0	0	0	08
9	DDR2 SDRAM FB-DIMM	0	0	0	0	1	0	0	1	09
10	DDR2 SDRAM FB-DIMM PROBE	0	0	0	0	1	0	1	0	0A
11	DDR3 SDRAM	0	0	0	0	1	0	1	1	0B
12	DDR4 SDRAM	0	0	0	0	1	1	0	0	0C
-	-	-	-	-	-	-	-	-	-	-
253	Reserved	1	1	1	1	1	1	0	1	FD
254	Reserved	1	1	1	1	1	1	1	0	FE
255	Reserved	1	1	1	1	1	1	1	1	FF

Byte 3 (0x003): Key Byte / Module Type

This byte is a Key Byte used to index the module specific section of the SPD from bytes 128~255. Byte 3 identifies the SDRAM memory module type which implies the width (D dimension) of the module. Other module physical characteristics, such as height (A dimension) or thickness (E dimension) are documented in the module specific section of the SPD. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

Bits 7~4	Bits 3~0
Reserved	**Module Type**
Reserved; must be coded as 0000	Bits [3, 2, 1, 0]: 0000 = Extended module type, see byte 15 (0x00F) 0001 = RDIMM 0010 = UDIMM 0011 = SO-DIMM 0100 = LRDIMM 0101 = Mini-RDIMM 0110 = Mini-UDIMM 0111 = Reserved 1000 = 72b-SO-RDIMM 1001 = 72b-SO-UDIMM 1011 - Reserved 1100 = 16b-SO-DIMM 1101 = 32b-SO-DIMM 1110 = Reserved 1111 = No base memory present (placeholder)
Base Module Type Definitions: RDIMM: Registered Dual In-Line Memory Module UDIMM: Unbuffered Dual In-Line Memory Module SO-DIMM: Unbuffered Small Outline Dual In-Line Memory Module, 64-bit data bus LRDIMM: Load Reduced Dual In-Line Memory Module Mini-RDIMM: Mini Registered Dual In-Line Memory Module Mini-UDIMM: Mini Unbuffered Dual In-Line Memory Module 72b-SO-RDIMM: Small Outline Registered Dual In-Line Memory Module, 72-bit data bus 72b-SO-UDIMM: Small Outline Unbuffered Dual In-Line Memory Module, 72-bit data bus 16b-SO-DIMM: Small Outline Unbuffered Dual In-Line Memory Module, 16-bit data bus 32b-SO-DIMM: Small Outline Unbuffered Dual In-Line Memory Module, 32-bit data bus	

Byte 4 (0x004): SDRAM Density and Banks

This byte defines the total density of the DDR4 SDRAM, in bits, and the number of internal banks and bank groups into which the memory array is divided. These values come from the DDR4 SDRAM data sheet.

Bits 7~6	Bits 5~4	Bits 3~0
Bank Group Bits	**Bank Address Bits[1]**	**Total SDRAM capacity, in megabits**
Bits [7, 6]: 00 = 0 (no bank groups) 01 = 1 (2 bank groups) 10 = 2 (4 bank groups) 11 = reserved	Bit [5, 4]: 00 = 2 (4 banks) 01 = 3 (8 banks) All others reserved	Bit [3, 2, 1, 0]: 0000 = 256 Mb 0001 = 512 Mb 0010 = 1 Gb 0011 = 2 Gb 0100 = 4 Gb 0101 = 8 Gb 0110 = 16 Gb 0111 = 32 Gb All others reserved
Note 1 Bank Address Bits determine the number of banks in each Bank Group.		

Byte 5 (0x005): SDRAM Addressing

This byte describes the row addressing and the column addressing in the SDRAM device. Bits 2~0 encode the number of column address bits, and bits 5~3 encode the number of row address bits. These values come from the DDR4 SDRAM data sheet.

Bits 7~6	Bits 5~3	Bits 2~0
Reserved	**Row Address Bits**	**Column Address Bits**
Reserved	Bit [5, 4, 3]: 000 = 12 001 = 13 010 = 14 011 = 15 100 = 16 101 = 17 110 = 18 All others reserved	Bit [2, 1, 0]: 000 = 9 001 = 10 010 = 11 011 = 12 All others reserved

Byte 6 (0x006): SDRAM Package Type

This byte describes the type of SDRAM Device on the module.

Bit 7	Bits 6~4	Bits 3~2	Bit 1~0
SDRAM Package Type	**Die Count**	**Reserved**	**Signal Loading[2]**
0 = Monolithic DRAM Device 1 = Non-Monolithic Device[1]	000 = Single die 001 = 2 die 010 = 3 die 011 = 4 die 100 = 5 die 101 = 6 die 110 = 7 die 111 = 8 die All others settings reserved.	00	00 = Not specified 01 = Multi load stack 10 = Single load stack (3DS) 11 = Reserved

Note 1 This includes Dual Die, Quad Die, Multi-Die, 3DS, or physically stacked devices - anything that is outside the standard monolithic device

Note 2 Refers to loading on signals at the SDRAM balls. Loading on certain signals (CKE, ODT, etc.) per specification of device stacking as defined in JESD79-4

Terminology:

SDRAM Package Type	Abbreviation	Description	# Electrical Loads ...			
			... On data, mask, and strobe signals	... On address and command signals	... On control signals except CKE	... On CKE signals
Monolithic	SDP	Single die package	1	1	1	1
Multi-load stack	DDP	Dual Die Package	2	2	1	1
	QDP	Quad Die Package	4	4	1	2
Single load stack	2H 3DS	Two SDRAM die single load stack	1	1	1	1
	3H 3DS	Three SDRAM die single load stack	1	1	1	1
	4H 3DS	Four SDRAM die single load stack	1	1	1	1
	5H 3DS	Five SDRAM die single load stack	1	1	1	1
	6H 3DS	Six SDRAM die single load stack	1	1	1	1
	7H 3DS	Seven SDRAM die single load stack	1	1	1	1
	8H 3DS	Eight SDRAM die single load stack	1	1	1	1

Byte 7 (0x007): SDRAM Optional Features

This byte defines support for certain SDRAM features. This value comes from the DDR4 SDRAM data sheet.

Bits 7~6	Bits 5~4	Bits 3~0
Reserved	**Maximum Activate Window (tMAW)**	**Maximum Activate Count (MAC)**
Reserved; must be coded as 0	Bits [5, 4]: 00 = 8192 * tREFI 01 = 4096 * tREFI 10 = 2048 * tREFI 11 = Reserved	Bits [3, 2, 1, 0] : 0000 = Untested MAC[1] 0001 = 700 K 0010 = 600 K 0011 = 500 K 0100 = 400 K 0101 = 300 K 0110 = 200 K 0111 = Reserved 1000 = Unlimited MAC[2] All other codes reserved
Note 1 Untested MAC means the device is not tested for tMAW and/or MAC; no particular value should be assumed. **Note 2** Unlimited MAC means there is no restriction to the number of activates to a given row in a refresh period providing DRAM timing requirements such as tRCmin and refresh requirements are not violated.		

Byte 8 (0x008): SDRAM Thermal and Refresh Options

This byte describes the module's supported operating temperature ranges and refresh options. These values come from the DDR4 SDRAM data sheet. Please refer to the DDR4 SDRAM data sheet (JESD79-4 or supplier data sheet) for a complete description of these options.

Bits 7~0
Reserved
Reserved; must be coded as 0x00

Byte 9 (0x009): Other SDRAM Optional Features

This byte defines support for certain SDRAM features. This value comes from the DDR4 SDRAM data sheet.

Bits 7~6	Bits 5~0
Post Package Repair (PPR)	**Reserved**
00: PPR not supported 01: Post package repair supported, one row per bank group 10: Reserved 11: Reserved	**Reserved; must be coded as 0**

Byte 10 (0x00A):

Reserved, must be coded as 0x00

Byte 11 (0x00B): Module Nominal Voltage, VDD

This byte describes the Voltage Level for DRAM and other components on the module, such as the register or memory buffer, if applicable. Note that SPDs or thermal sensor components are on the VDDSPD supply and are not affected by this byte. Systems are required to parse this byte prior to applying power to the DRAMs to avoid damage to the module or to the system. Systems that do not support the required voltages must reject the module and must not apply power to the DRAMs.

'Operable' is defined as the VDD voltage at which module operation is allowed using the performance values programmed in the SPD.

'Endurant' is defined as the VDD voltage at which the module may be powered without adversely affecting the life expectancy or reliability. Operation is not supported at this voltage.

Byte 11: Module Nominal Voltage, VDD						
Reserved	**DRAM VDD TBD2 V**		**DRAM VDD TBD1 V**		**DRAM VDD 1.2 V**	
Bits 7~6	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Reserved; 00	0 = not endurant 1 = endurant	0 = not operable 1 = operable	0 = not endurant 1 = endurant	0 = not operable 1 = operable	0 = not endurant 1 = endurant	0 = not operable 1 = operable
Note 1 Systems are required to verify valid supply voltages before applying power to the DRAMs.						

Examples:

A value on bits 5~0 of 000011 defines DRAM support of a nominal operable voltage of 1.2 V only.

A value on bits 5~0 of 001111 defines DRAM support of a nominal operable voltage of TBD1 V or 1.2 V.

A value on bits 5~0 of 001110 defines DRAM support of a nominal operable voltage of TBD1 V but DRAMs are endurant at 1.2 V, while not operable at 1.2 V.

A value on bits 5~0 of 111000 defines DRAM support of a nominal operable voltage of TBD2 V, endurant but not operable at TBD1 V, and neither operable nor endurant at 1.2 V.

Byte 12 (0x00C): Module Organization

This byte describes the organization of the SDRAM module. Bits 2~0 encode the device width of the SDRAM devices. Bits 5~3 encode the number of package ranks on the module.

Bits 7~6	Bits 5~3	Bits 2~0
Reserved	**Number of Package Ranks per DIMM**	**SDRAM Device Width**
Reserved; 00	Bit [5, 4, 3] : 000 = 1 Package Rank 001 = 2 Package Ranks 010 = 3 Package Ranks 011 = 4 Package Ranks All others reserved	Bit [2, 1, 0] : 000 = 4 bits 001 = 8 bits 010 = 16 bits 011 = 32 bits All others reserved

“Package ranks per DIMM” refers to the collections of devices on the module sharing common chip select signals (across the data width of the DIMM), either from the edge connector for unbuffered modules or from the outputs of a registering clock driver for RDIMMs and LRDIMMs.

“Logical rank” refers the individually addressable die in a 3DS stack and has no meaning for monolithic or multi-load stacked SDRAMs; however, for the purposes of calculating the capacity of the module, one should treat monolithic and multi-load stack SDRAMs as having one logical rank per package rank.

SDRAM Package Type	# Package Ranks per DIMM	# Logical Ranks per Package Rank (for calculation only)	# Logical Ranks per DIMM
SDP	1	1	1
	2		2
DDP	2		2
	4		4
QDP	4		4
2H 3DS	1	2	2
	2		4
4H 3DS	1	4	4
	2		8
8H 3DS	1	8	8
	2		16
Logical Ranks per DIMM = # Package Ranks per DIMM * # Logical Ranks per Package Rank			

Byte 13 (0x00D): Module Memory Bus Width

This byte describes the width of the SDRAM memory bus on the module. Bits 2~0 encode the primary bus width. Bits 4~3 encode the bus extensions such as parity or ECC.

Bits 7~5	Bits 4~3	Bits 2~0
Reserved	**Bus width extension, in bits**	**Primary bus width, in bits**
00	Bit [4, 3] : 000 = 0 bits (no extension) 001 = 8 bits All others reserved	Bit [2, 1, 0] : 000 = 8 bits 001 = 16 bits 010 = 32 bits 011 = 64 bits All others reserved

Examples:

- 64 bit primary bus, no parity or ECC (64 bits total width): xxx 000 011
- 64 bit primary bus, with 8 bit ECC (72 bits total width): xxx 001 011

Calculating Module Capacity

The total memory capacity of the module may be calculated from SPD values. For example, to calculate the total capacity, in megabytes or gigabytes, of a typical module:

Total = SDRAM Capacity ÷ 8 * Primary Bus Width ÷ SDRAM Width * Logical Ranks per DIMM

where:

- SDRAM Capacity = SPD byte 4 bits 3~0
- Primary Bus Width = SPD byte 13 bits 2~0
- SDRAM Width = SPD byte 12 bits 2~0
- Logical Ranks per DIMM =

  for SDP, DDP, QDP: = SPD byte 12 bits 5~3

  for 3DS: = SPD byte 12 bits 5~3 times SPD byte 6 bits 6~4

Examples:

2 package ranks per DIMM using monolithic SDRAMs, 2 Gb per die, with x4 organization on a module with a 64 bit primary bus:

- Total = 2 Gb ÷ 8 * 64 ÷ 4 * 2 * 1 = 8 GB

2 package ranks per DIMM using DDP SDRAMs, 4 Gb per die, with x4 organization on a module with a 64 bit primary bus:

- Total = 4 Gb ÷ 8 * 64 ÷ 4 * 2 = 16 GB

2 package ranks per DIMM using 4H 3DS SDRAMs, 2 Gb per die, having a x8 organization on a module with a 64 bit primary bus:

- Total = 2 Gb ÷ 8 * 64 ÷ 8 * 2 * 4 = 16 GB

Commonly, parity or ECC are not counted in total module capacity, though they can also be included by adding the bus width extension in SPD byte 13 bits 4~3 to the primary bus width in the previous examples.

Byte 14 (0x00E): Module Thermal Sensor

This byte describes the module's supported thermal options.

Bit 7	Bits 6~0
Thermal Sensor[1]	**Reserved**
0 = Thermal sensor not incorporated onto this assembly 1 = Thermal sensor incorporated onto this assembly	0 = Undefined All others settings to be defined.
Note 1 Thermal sensor compliant with TSE2004av specifications.	

Byte 15 (0x00F): Extended Module Type

This byte extends the module type field of byte 3. Used when byte 3 bits 3~0 = 0000.

Bit 7~4	Bits 3~0
Reserved	**Extended Base Module Type**
Reserved; must be coded as 0000	Bits [3, 2, 1, 0]: 0000 = Reserved; must be coded as 0000 ... 1111 = Reserved; must be coded as 0000

Byte 16 (0x010):

Reserved, must be coded as 0x00

Byte 17 (0x011): Timebases

This byte defines a value in picoseconds that represents the fundamental timebase for fine grain and medium grain timing calculations. These values are used as a multiplier for formulating subsequent timing parameters.

Bits 7~4	Bits 3~2	Bits 1~0
Reserved	**Medium Timebase (MTB)**	**Fine Timebase (FTB)**
Reserved; 0000	Bits [3, 2]: 00 = 125 ps All other values reserved	Bits [0, 1]: 00 = 1 ps All other values reserved

Relating the MTB and FTB

When a timing value tXX cannot be expressed by an integer number of MTB units, the SPD must be encoded using both the MTB and FTB. The Fine Offsets are encoded using a two's complement value which, when multiplied by the FTB yields a positive or negative correction factor. Typically, for safety and for legacy compatibility, the MTB portion is rounded UP and the FTB correction is a negative value. The general algorithm for programming SPD values is:

```
Temp_val = tXX / MTB                          // Calculate as real number
Remainder = Temp_val modulo 1                 // Determine if integer # MTBs
Fine_Correction = 1 - Remainder               // If needed, what correction
if (Remainder == 0) then                      // Integer # MTBs?
        tXX(MTB) = Temp_val                   // Convert to integer
        tXX(FTB) = 0                          // No correction needed
else                                          // Needs correction
        tXX(MTB) = ceiling (Temp_val)         // Round up for safety in legacy systems
        tXX(FTB) = Fine_Correction * MTB / FTB // Correction is negative offset
endif
```

To recalculate the value of tXX from the SPD values, a general formula BIOSes may use is:

tXX = tXX(MTB) * MTB + tXX(FTB) * FTB

Example:

t_{CKAVG}min SPD Calculations Using MTB and FTB			
Speed Bin	**t_{CKAVG}min Value Decimal**	**SPD byte 18 Decimal (Hexadecimal)**	**SPD byte 125 Decimal (Hexadecimal)**
DDR4-1866	1.071 ns	9 (0x09)	-54 (0xCA)
	=	(9 * 0.125) + (-54 * 0.001)	
Note 1 Examples assume MTB of 0.125 ns and FTB of 0.001 ns			

Timing parameters using both MTB and FTB are:

Table 2 — MTB and FTB Timing Parameters

Parameter	MTB Byte(s)	FTB Byte
t_{CKAVG}min	18 (0x012)	125 (0x07D)
t_{CKAVG}max	19 (0x013)	124 (0x07C)
t_{AA}min	24 (0x018)	123 (0x07B)
t_{RCD}min	25 (0x019)	122 (0x07A)
t_{RP}min	26 (0x01A)	121 (0x079)
t_{RC}min	27, 29 (0x01B, 0x01D)	120 (0x078)
t_{RRD_S}min	39 (0x027)	119 (0x077)
t_{RRD_L}min	40 (0x028)	118 (0x076)

The encoding of two's complement fine timebase offsets:

Coding		Value (Dec)	Value (Hex)	FTB Timebase
Bit 7	Bits 6~0			1 ps
0	1111111	+127	7F	+127 ps
0	1111110	+126	7E	+126 ps
...	...	...	...	
0	0000001	+1	01	+1 ps
0	0000000	0	00	0
1	1111111	-1	FF	-1 ps
1	1111110	-2	FE	-2 ps
...	...	...	...	
1	0000000	-128	80	-128 ps

Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33... MHz, or a clock period of 1.0714... ns. Similarly, a system with a memory clock frequency of 1066.66... MHz yields mathematically a clock period of 0.9375... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the SPD establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of memory module performance without violating device parameters. These algorithms rely on results that are within guardbands on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

1. Clock periods such as t_{CKAVG}min are rounded to the nearest picosecond of accuracy; for example, 0.9375... ns is rounded to 938 ps and 1.0714... ns is rounded to 1071 ps.
2. Parameters programmed in systems in numbers of clocks (nCK) but expressed in the SPD in units of time (ns or ps) are divided by the clock period, a guardband factor of 0.01 clocks is subtracted, then the result is rounded up to the nearest integer number of clocks. Examples:

DDR4 Bin	Parameter	Value	@ t_{CKAVG}-min	Temp Result	- Guardband	Rounding Result
		ps	ps	nCK	nCK	nCK
1600	t_{RRD_L}min	7500	1250	6.000	5.990	6
1600	t_{RRD_L}min	7500	1071	7.002	6.992	7
2133	t_{RRD_L}min	6400	1250	5.120	5.110	6
1866	t_{RRD_L}min	5300	1071	4.948	4.938	5

Byte 18 (0x012): SDRAM Minimum Cycle Time (t_{CKAVG}min)

This byte defines the minimum cycle time for the SDRAM module, in medium timebase (MTB) units. This number applies to all applicable components on the module. This byte applies to SDRAM and support components as well as the overall capability of the DIMM. This value comes from the DDR4 SDRAM and support component data sheets.

Bits 7~0
Minimum SDRAM Cycle Time (t_{CKAVG}min) MTB Units
Values defined from 1 to 255

If t_{CKAVG}min cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{CKAVG}min (SPD byte 125) used for correction to get the actual value.

Examples:

t_{CKAVG}min (MTB units)		MTB (ns)	t_{CKAVG}min Offset (FTB units)[1]		FTB (ns)	t_{CKAVG}min Result (ns)	Use
10	0x0A	0.125	0	0	0.001	1.25	DDR4-1600 (800 MHz clock)
9	0x09	0.125	-54	0xCA	0.001	1.071	DDR4-1866 (933 MHz clock)
8	0x08	0.125	**-63**	**0xC1**	0.001	0.938	DDR4-2133 (1067 MHz clock)
7	0x07	0.125	-42	0xD6	0.001	0.833	DDR4-2400 (1200 MHz clock)
6	0x06	0.125	0	0	0.001	0.750	DDR4-2666 (1333 MHz clock)
5	0x05	0.125	0	0	0.001	0.625	DDR4-3200 (1600 MHz clock)
Note 1 See SPD byte 125.							

Byte 19 (0x013): SDRAM Maximum Cycle Time (t_{CKAVG}max)

This word defines the maximum cycle time for the SDRAM module, in medium timebase (MTB) units This number applies to all applicable components on the module. This byte applies to SDRAM and support components as well as the overall capability of the DIMM. This value comes from the DDR4 SDRAM and support component data sheets.

Bits 7~0
Minimum SDRAM Cycle Time (t_{CKAVG}max) MTB Units
Values defined from 1 to 255

If t_{CKAVG}max cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{CKAVG}max (SPD byte 124) used for correction to get the actual value.

Examples:

t_{CKAVG}max (MTB units)		MTB (ns)	t_{CKAVG}max Offset (FTB units)[1]		FTB (ns)	t_{CKAVG}max Result (ns)	Use
12	0x0C	0.125	0	0	0.001	1.500	DDR4-1600 (800 MHz clock)
12	0x0C	0.125	0	0	0.001	1.500	DDR4-1866 (933 MHz clock)
12	0x0C	0.125	0	0	0.001	1.500	DDR4-2133 (1067 MHz clock)
12	0x0C	0.125	0	0	0.001	1.500	DDR4-2400 (1200 MHz clock)
		0.125			0.001	tbd	DDR4-2666 (1333 MHz clock)
		0.125			0.001	tbd	DDR4-3200 (1600 MHz clock)
Note 1 See SPD byte 124.							

Byte 20 (0x014): CAS Latencies Supported, First Byte
Byte 21 (0x015): CAS Latencies Supported, Second Byte
Byte 22 (0x016): CAS Latencies Supported, Third Byte
Byte 23 (0x017): CAS Latencies Supported, Fourth Byte

These bytes define which CAS Latency (CL) values are supported. The range is from CL = 7 through CL = 24 with one bit per possible CAS Latency. A 1 in a bit position means that CL is supported, a 0 in that bit position means it is not supported. These values come from the DDR4 SDRAM data sheet, JESD79-4.

Byte 20: CAS Latencies Supported, First Byte							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CL = 14	**CL = 13**	**CL = 12**	**CL = 11**	**CL = 10**	**CL = 9**	**CL = 8**	**CL = 7**
0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Byte 21: CAS Latencies Supported, Second Byte							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CL = 22	**CL = 21**	**CL = 20**	**CL = 19**	**CL = 18**	**CL = 17**	**CL = 16**	**CL = 15**
0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Byte 22: CAS Latencies Supported, Third Byte							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Reserved	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**CL = 24**	**CL = 23**
0	0	0	0	0	0	0 or 1	0 or 1
Byte 23: CAS Latencies Supported, Fourth Byte							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Reserved	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
0	0	0	0	0	0	0	0
For each bit position, 0 means this CAS Latency is not supported, 1 means this CAS Latency is supported.							

Example:

Byte 20 = 0xB4 (= 1011 0100) -- first byte
Byte 21 = 0x05 (= 0000 0101) -- second byte
Byte 22 = 0x00 (= 0000 0000) -- third byte
Byte 23 = 0x00 (= 0000 0000) -- fourth byte

CAS Latencies	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**
CL Mask	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**0**	**0**
CAS Latencies	**tbd**	**tbd**	**tbd**	**tbd**	**tbd**	**tbd**	**tbd**	**tbd**	**tbd**	**tbd**	**tbd**	**tbd**	**tbd**	**tbd**	**24**	**23**
CL Mask	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Results: Actual CAS Latencies supported = 9, 11, 12, 14, 15, 17

Byte 24 (0x018): Minimum CAS Latency Time (t_{AA}min)

This word defines the minimum CAS Latency in medium timebase (MTB) units. This value comes from the DDR4 SDRAM data sheet.

Bits 7~0
Minimum SDRAM CAS Latency Time (t_{AA}min) MTB Units
Values defined from 1 to 255

If t_{AA}min cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{AA}min (SPD byte 123) used for correction to get the actual value.

Examples:

t_{AA}min (MTB units)		MTB (ns)	t_{AA}min Offset (FTB units)[1]		FTB (ns)	t_{AA}min Result (ns)	Use
100	0x64	0.125	0	0	0.001	12.50	DDR4-1600J (800 MHz clock)
110	0x6E	0.125	0	0	0.001	13.75	DDR4-1600K (800 MHz clock)
108	0x6C	0.125	0	0	0.001	13.50	DDR4-1600K (800 MHz clock) downbin[2]
120	0x78	0.125	0	0	0.001	15.00	DDR4-1600L (800 MHz clock)
103	0x67	0.125	-26	0xE6	0.001	12.85	DDR4-1866L (933 MHz clock)
112	0x70	0.125	-81	0xAF	0.001	13.92	DDR4-1866M (933 MHz clock)
108	0x6C	0.125	0	0	0.001	13.50	DDR4-1866M (933 MHz clock) downbin[2]
120	0x78	0.125	0	0	0.001	15.00	DDR4-1866N (933 MHz clock)
106	0x6A	0.125	-120	0x88	0.001	13.13	DDR4-2133N (1066 MHz clock)
113	0x71	0.125	-65	0xBF	0.001	14.06	DDR4-2133P (1066 MHz clock)
108	0x6C	0.125	0	0	0.001	13.50	DDR4-2133P (1066 MHz clock) downbin[2]
120	0x78	0.125	0	0	0.001	15.00	DDR4-2133R (1066 MHz clock)
100	0x64	0.125	0	0	0.001	12.50	DDR4-2400P (1200 MHz clock)
107	0x6B	0.125	-55	0xC9	0.001	13.32	DDR4-2400R (1200 MHz clock)
120	0x78	0.125	0	0	0.001	15.00	DDR4-2400U (1200 MHz clock)
		0.125			0.001	tbd	DDR4-2666 (1333 MHz clock)
		0.125			0.001	tbd	DDR4-3200 (1600 MHz clock)
120	0x78	0.125	0	0	0.001	15.00	DDR4-1600J-3DS2B
130	0x82	0.125	0	0	0.001	16.25	DDR4-1600K-3DS2B
140	0x8C	0.125	0	0	0.001	17.50	DDR4-1600L-3DS2B
120	0x78	0.125	0	0	0.001	15.00	DDR4-1866L-3DS2B
129	0x81	0.125	-55	0xC9	0.001	16.07	DDR4-1866M-3DS2B
129	0x81	0.125	-55	0xC9	0.001	16.07	DDR4-1866M-3DS2B (downbin)
138	0x8A	0.125	-110	0x92	0.001	17.14	DDR4-1866N-3DS2B
120	0x78	0.125	0	0	0.001	15.00	DDR4-2133N-3DS2B
120	0x78	0.125	0	0	0.001	15.00	DDR4-2133N-3DS2B (downbin)
136	0x88	0.125	-121	0x87	0.001	16.88	DDR4-2133R-3DS2A
151	0x97	0.125	-115	0x8D	0.001	18.76	DDR4-2133R-3DS4A
138	0x8A	0.125	-110	0x92	0.001	17.14	DDR4-2133R-3DS4A (downbin)
120	0x78	0.125	0	0	0.001	15.00	DDR4-2400N-3DS3B
134	0x86	0.125	-80	0xB0	0.001	16.67	DDR4-2400U-3DS2A
147	0x93	0.125	-46	0xD2	0.001	18.33	DDR4-2400U-3DS4A
138	0x8A	0.125	-110	0x92	0.001	17.14	DDR4-2400U-3DS4A (downbin)

Note 1 See SPD byte 123
Note 2 Refer to device data sheet for downbin support details.

Byte 25 (0x019): Minimum RAS to CAS Delay Time (t_{RCD}min)

This word defines the minimum SDRAM RAS to CAS Delay Time in fine timebase (FTB) units. This value comes from the DDR4 SDRAM data sheet.

Bits 7~0
Byte 25: Minimum SDRAM RAS to CAS Delay Time (t_{RCD}min) FTB Units
Values defined from 1 to 255

If t_{RCD}min cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{RCD}min (SPD byte 122) used for correction to get the actual value
Examples:

t_{RCD}min (MTB units)		MTB (ns)	t_{RCD}min Offset (FTB units)[1]		FTB (ns)	t_{RCD}min Result (ns)	Use
100	0x64	0.125	0	0	0.001	12.50	DDR4-1600J (800 MHz clock)
110	0x6E	0.125	0	0	0.001	13.75	DDR4-1600K (800 MHz clock)
108	0x6C	0.125	0	0	0.001	13.50	DDR4-1600K (800 MHz clock) downbin[2]
120	0x78	0.125	0	0	0.001	15.00	DDR4-1600L (800 MHz clock)
103	0x67	0.125	-26	0xE6	0.001	12.85	DDR4-1866L (933 MHz clock)
112	0x70	0.125	-81	0xAF	0.001	13.92	DDR4-1866M (933 MHz clock)
108	0x6C	0.125	0	0	0.001	13.50	DDR4-1866M (933 MHz clock) downbin2
120	0x78	0.125	0	0	0.001	15.00	DDR4-1866N (933 MHz clock)
106	0x6A	0.125	-120	0x88	0.001	13.13	DDR4-2133N (1066 MHz clock)
113	0x71	0.125	-65	0xBF	0.001	14.06	DDR4-2133P (1066 MHz clock)
108	0x6C	0.125	0	0	0.001	13.50	DDR4-2133P (1066 MHz clock) downbin2
120	0x78	0.125	0	0	0.001	15.00	DDR4-2133R (1066 MHz clock)
100	0x64	0.125	0	0	0.001	12.50	DDR4-2400P (1200 MHz clock)
107	0x6B	0.125	-55	0xC9	0.001	13.32	DDR4-2400R (1200 MHz clock)
120	0x78	0.125	0	0	0.001	15.00	DDR4-2400U (1200 MHz clock)
		0.125			0.001	tbd	DDR4-2666 (1333 MHz clock)
		0.125			0.001	tbd	DDR4-3200 (1600 MHz clock)
110	0x6E	0.125	0	0	0.001	13.75	DDR4-1600J-3DS2B
120	0x78	0.125	0	0	0.001	15.00	DDR4-1600K-3DS2B
130	0x82	0.125	0	0	0.001	16.25	DDR4-1600L-3DS2B
112	0x70	0.125	-81	0xAF	0.001	13.92	DDR4-1866L-3DS2B
120	0x78	0.125	0	0	0.001	15.00	DDR4-1866M-3DS2B
120	0x78	0.125	0	0	0.001	15.00	DDR4-1866M-3DS2B (downbin)
129	0x81	0.125	-55	0xC9	0.001	16.07	DDR4-1866N-3DS2B
113	0x71	0.125	-65	0xBF	0.001	14.06	DDR4-2133N-3DS2B
112	0x70	0.125	-81	0xAF	0.001	13.92	DDR4-2133N-3DS2B (downbin)
120	0x78	0.125	0	0	0.001	15.00	DDR4-2133R-3DS2A
120	0x78	0.125	0	0	0.001	15.00	DDR4-2133R-3DS4A
120	0x78	0.125	0	0	0.001	15.00	DDR4-2133R-3DS4A (downbin)
107	0x6B	0.125	-45	0xD3	0.001	13.33	DDR4-2400N-3DS3B
120	0x78	0.125	0	0	0.001	15.00	DDR4-2400U-3DS2A
120	0x78	0.125	0	0	0.001	15.00	DDR4-2400U-3DS4A
120	0x78	0.125	0	0	0.001	15.00	DDR4-2400U-3DS4A (downbin)

Note 1 See SPD byte 122
Note 2 Refer to device data sheet for downbin support details.

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Byte 26 (0x01A): Minimum Row Precharge Delay Time (t_{RP}min)

This word defines the minimum SDRAM Row Precharge Delay Time in medium timebase (MTB) units. This value comes from the DDR4 SDRAM data sheet.

Bits 7~0
Minimum Row Precharge Time (t_{RP}min) MTB Units
Values defined from 1 to 255

If t_{RP}min cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{RP}min (SPD byte 121) used for correction to get the actual value.

Examples:

t_{RP}min (MTB units)		MTB (ns)	t_{RP}min Offset (FTB units)[1]		FTB (ns)	t_{RP}min Result (ns)	Use
100	0x64	0.125	0	0	0.001	12.50	DDR4-1600J (800 MHz clock)
110	0x6E	0.125	0	0	0.001	13.75	DDR4-1600K (800 MHz clock)
108	0x6C	0.125	0	0	0.001	13.50	DDR4-1600K (800 MHz clock) downbin[2]
120	0x78	0.125	0	0	0.001	15.00	DDR4-1600L (800 MHz clock)
103	0x67	0.125	-26	0xE6	0.001	12.85	DDR4-1866L (933 MHz clock)
112	0x70	0.125	-81	0xAF	0.001	13.92	DDR4-1866M (933 MHz clock)
108	0x6C	0.125	0	0	0.001	13.50	DDR4-1866M (933 MHz clock) downbin[2]
120	0x78	0.125	0	0	0.001	15.00	DDR4-1866N (933 MHz clock)
106	0x6A	0.125	-120	0x88	0.001	13.13	DDR4-2133N (1066 MHz clock)
113	0x71	0.125	-65	0xBF	0.001	14.06	DDR4-2133P (1066 MHz clock)
108	0x6C	0.125	0	0	0.001	13.50	DDR4-2133P (1066 MHz clock) downbin[2]
120	0x78	0.125	0	0	0.001	15.00	DDR4-2133R (1066 MHz clock)
100	0x64	0.125	0	0	0.001	12.50	DDR4-2400P (1200 MHz clock)
107	0x6B	0.125	-55	0xC9	0.001	13.32	DDR4-2400R (1200 MHz clock)
120	0x78	0.125	0	0	0.001	15.00	DDR4-2400U (1200 MHz clock)
		0.125			0.001	tbd	DDR4-2666 (1333 MHz clock)
		0.125			0.001	tbd	DDR4-3200 (1600 MHz clock)
100	0x64	0.125	0	0	0.001	12.50	DDR4-1600J-3DS2B
110	0x6E	0.125	0	0	0.001	13.75	DDR4-1600K-3DS2B
120	0x78	0.125	0	0	0.001	15.00	DDR4-1600L-3DS2B
103	0x67	0.125	-26	0xE6	0.001	12.85	DDR4-1866L-3DS2B
112	0x70	0.125	-81	0xAF	0.001	13.92	DDR4-1866M-3DS2B
110	0x6E	0.125	0	0	0.001	13.75	DDR4-1866M-3DS2B (downbin)
120	0x78	0.125	0	0	0.001	15.00	DDR4-1866N-3DS2B
106	0x6A	0.125	-120	0x88	0.001	13.13	DDR4-2133N-3DS2B
103	0x67	0.125	-26	0xE6	0.001	12.85	DDR4-2133N-3DS2B (downbin)
120	0x78	0.125	0	0	0.001	15.00	DDR4-2133R-3DS2A
120	0x78	0.125	0	0	0.001	15.00	DDR4-2133R-3DS4A
120	0x78	0.125	0	0	0.001	15.00	DDR4-2133R-3DS4A (downbin)
100	0x64	0.125	0	0	0.001	12.50	DDR4-2400N-3DS3B
120	0x78	0.125	0	0	0.001	15.00	DDR4-2400U-3DS2A
120	0x78	0.125	0	0	0.001	15.00	DDR4-2400U-3DS4A
120	0x78	0.125	0	0	0.001	15.00	DDR4-2400U-3DS4A (downbin)

Note 1 See SPD byte 121
Note 2 Device supports downbinning in lower frequency applications; see supplier data sheet

Byte 27 (0x01B): Upper Nibbles for t_{RAS}min and t_{RC}min

This byte defines the most significant nibbles for the values of t_{RAS}min (byte 28) and t_{RC}min (byte 29). These values come from the DDR4 SDRAM data sheet.

Bits 7~4	Bits 3~0
t_{RC}min Most Significant Nibble	**t_{RAS}min Most Significant Nibble**
See Byte 28 description	See Byte 29 description

Byte 28 (0x01C): Minimum Active to Precharge Delay Time (t_{RAS}min), Least Significant Byte

The lower nibble of Byte 27 and the contents of Byte 28 combined create a 12-bit value which defines the minimum SDRAM Active to Precharge Delay Time in medium timebase (MTB) units. The most significant bit is Bit 3 of Byte 27, and the least significant bit is Bit 0 of Byte 28. This value comes from the DDR4 SDRAM data sheet.

Byte 27 Bits 3~0, Byte 28 Bits 7~0
Minimum Active to Precharge Time (t_{RAS}min) MTB Units
Values defined from 1 to 4095

Examples:

t_{RAS}min (MTB units)		MTB (ns)	t_{RAS}min Result (ns)	Use
280	0x118	0.125	35	DDR4-1600 (800 MHz clock)
272	0x110	0.125	34	DDR4-1866 (933 MHz clock)
264	0x108	0.125	33	DDR4-2133 (1066 MHz clock)
256	0x100	0.125	32	DDR4-2400 (1200 MHz clock)
		0.125	TBD	DDR4-2666 (1333 MHz clock)
		0.125	TBD	DDR4-3200 (1600 MHz clock)

Byte 29 (0x01D): Minimum Active to Active/Refresh Delay Time (t_{RC}min), Least Significant Byte

The upper nibble of Byte 27 and the contents of Byte 29 combined create a 12-bit value which defines the minimum SDRAM Active to Active/Refresh Delay Time in medium timebase (MTB) units. The most significant bit is Bit 7 of Byte 27, and the least significant bit is Bit 0 of Byte 29. This value comes from the DDR4 SDRAM data sheet.

Byte 27 Bits 7~4, Byte 29 Bits 7~0
Minimum Active to Active/Refresh Time (t_{RC}min) MTB Units
Values defined from 1 to 4095

If t_{RC}min cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{RC}min (SPD byte 120) used for correction to get the actual value.

Examples:

t_{RC}min (MTB units)		MTB (ns)	t_{RC}min Offset (FTB units)[1]		FTB (ns)	t_{RC}min Result (ns)	Use
380	0x17C	0.125	0	0	0.001	47.50	DDR4-1600J (800 MHz clock)
390	0x186	0.125	0	0	0.001	48.75	DDR4-1600K (800 MHz clock)
388	0x184	0.125	0	0	0.001	48.50	DDR4-1600K (800 MHz clock) downbin[2]
400	0x190	0.125	0	0	0.001	50.00	DDR4-1600L (800 MHz clock)
375	0x177	0.125	-25	0xE7	0.001	46.85	DDR4-1866L (933 MHz clock)
384	0x180	0.125	-80	0xB0	0.001	47.92	DDR4-1866M (933 MHz clock)
380	0x17C	0.125	0	0	0.001	47.50	DDR4-1866M (933 MHz clock) downbin[2]
392	0x188	0.125	0	0	0.001	49.00	DDR4-1866N (933 MHz clock)
370	0x172	0.125	-120	0x88	0.001	46.13	DDR4-2133N (1066 MHz clock)
377	0x179	0.125	-65	0xBF	0.001	47.06	DDR4-2133P (1066 MHz clock)
372	0x174	0.125	0	0	0.001	46.50	DDR4-2133P (1066 MHz clock) downbin[2]
384	0x180	0.125	0	0	0.001	48.00	DDR4-2133R (1066 MHz clock)
356	0x164	0.125	0	0	0.001	44.50	DDR4-2400P (1200 MHz clock)
363	0x16B	0.125	-55	0xC9	0.001	45.32	DDR4-2400R (1200 MHz clock)
376	0x178	0.125	0	0	0.001	47.00	DDR4-2400U (1200 MHz clock)
380	0x17C	0.125	0	0	0.001	47.50	DDR4-1600J-3DS2B
390	0x186	0.125	0	0	0.001	48.75	DDR4-1600K-3DS2B
400	0x190	0.125	0	0	0.001	50.00	DDR4-1600L-3DS2B
375	0x177	0.125	-25	0xE7	0.001	46.85	DDR4-1866L-3DS2B
384	0x180	0.125	-80	0xB0	0.001	47.92	DDR4-1866M-3DS2B
384	0x180	0.125	-80	0xB0	0.001	47.92	DDR4-1866M-3DS2B (downbin)
392	0x188	0.125	0	0	0.001	49.00	DDR4-1866N-3DS2B
370	0x172	0.125	-120	0x88	0.001	46.13	DDR4-2133N-3DS2B
370	0x172	0.125	-120	0x88	0.001	46.13	DDR4-2133N-3DS2B (downbin)
384	0x180	0.125	0	0	0.001	48.00	DDR4-2133R-3DS2A
384	0x180	0.125	0	0	0.001	48.00	DDR4-2133R-3DS4A
384	0x180	0.125	0	0	0.001	48.00	DDR4-2133R-3DS4A (downbin)
356	0x164	0.125	0	0	0.001	44.50	DDR4-2400N-3DS3B
376	0x178	0.125	0	0	0.001	47.00	DDR4-2400U-3DS2A
376	0x178	0.125	0	0	0.001	47.00	DDR4-2400U-3DS4A
376	0x178	0.125	0	0	0.001	47.00	DDR4-2400U-3DS4A (downbin)

Note 1 See SPD byte 120
Note 2 Device supports downbinning in lower frequency applications; see supplier data sheet

Byte 30 (0x01E): Minimum Refresh Recovery Delay Time (t_{RFC1}min), LSB
Byte 31 (0x01F): Minimum Refresh Recovery Delay Time (t_{RFC1}min), MSB

This word defines the minimum SDRAM Refresh Recovery Time Delay in medium timebase (MTB) units. These values come from the DDR4 SDRAM data sheet.

Minimum SDRAM Refresh Recovery Delay Time (t_{RFC1}min) MTB Units	
Byte 30	**Byte 31**
Bits 15~8	**Bits 7~0**
Values defined from 1 to 65535	

Examples:

t_{RFC1}min (MTB units)		MTB (ns)	t_{RFC1}min Result (ns)	Use
1280	0x0500	0.125	160	2 Gb DDR4 SDRAM
2080	0x0820	0.125	260	4 Gb DDR4 SDRAM
2800	0x0AF0	0.125	350	8 Gb DDR4 SDRAM
		0.125	TBD	16 Gb DDR4 SDRAM

Byte 32 (0x020): Minimum Refresh Recovery Delay Time (t_{RFC2}min), LSB
Byte 33 (0x021): Minimum Refresh Recovery Delay Time (t_{RFC2}min), MSB

This word defines the minimum SDRAM Refresh Recovery Time Delay in medium timebase (MTB) units. These values come from the DDR4 SDRAM data sheet.

Minimum SDRAM Refresh Recovery Delay Time (t_{RFC2}min) MTB Units	
Byte 32	**Byte 33**
Bits 15~8	**Bits 7~0**
Values defined from 1 to 65535	

Examples:

t_{RFC2}min (MTB units)		MTB (ns)	t_{RFC2}min Result (ns)	Use
880	0x0370	0.125	110	2 Gb DDR4 SDRAM
1280	0x0500	0.125	160	4 Gb DDR4 SDRAM
2080	0x0820	0.125	260	8 Gb DDR4 SDRAM
		0.125	TBD	16 Gb DDR4 SDRAM

Byte 34 (0x022): Minimum Refresh Recovery Delay Time (t_{RFC4}min), LSB
Byte 35 (0x023): Minimum Refresh Recovery Delay Time (t_{RFC4}min), MSB

This word defines the minimum SDRAM Refresh Recovery Time Delay in medium timebase (MTB) units. These values come from the DDR4 SDRAM data sheet.

Minimum SDRAM Refresh Recovery Delay Time (t_{RFC4}min) MTB Units	
Byte 34	**Byte 35**
Bits 15~8	**Bits 7~0**
Values defined from 1 to 65535	

Examples:

t_{RFC4}min (MTB units)		**MTB (ns)**	**t_{RFC4}min Result (ns)**	**Use**
720	0x02D0	0.125	90	2 Gb DDR4 SDRAM
880	0x0370	0.125	110	4 Gb DDR4 SDRAM
1280	0x0500	0.125	160	8 Gb DDR4 SDRAM
		0.125	TBD	16 Gb DDR4 SDRAM

Byte 36 (0x024): Upper Nibble for t_{FAW}

This byte defines the most significant nibble for the value of t_{FAW} (SPD byte 37). This value comes from the DDR4 SDRAM data sheet.

Bits 7 ~ 4	**Bits 3 ~ 0**
Reserved	**t_{FAW} Most Significant Nibble**
Reserved	See Byte 38 description

Byte 37 (0x025): Minimum Four Activate Window Delay Time (t_{FAW}min), Least Significant Byte

The lower nibble of Byte 36 and the contents of Byte 37 combined create a 12-bit value which defines the minimum SDRAM Four Activate Window Delay Time in medium timebase (MTB) units. This value comes from the DDR4 SDRAM data sheet. The value of this number may be dependent on the SDRAM page size; please refer to the DDR4 SDRAM data sheet section on Addressing to determine the page size for these devices.

Byte 36 Bits 3 ~ 0, Byte 37 Bits 7 ~ 0
Minimum Four Activate Window Delay Time (t_{FAW}) MTB Units
Values defined from 1 to 4095

Examples:

tFAW (MTB units)		Timebase (ns)	tFAW Result (ns)	Use
280	0x118	0.125	35	Example: DDR4-1600, 2 KB page size
200	0x0C8	0.125	25	Example: DDR4-1600, 1 KB page size
160	0x0A0	0.125	20	Example: DDR4-1600, 1/2 KB page size
240	0x0F0	0.125	30	Example: DDR4-1866, 2 KB page size
184	0x0B8	0.125	23	Example: DDR4-1866, 1 KB page size
136	0x088	0.125	17	Example: DDR4-1866, 1/2 KB page size
240	0x0F0	0.125	30	Example: DDR4-2133, 2 KB page size
168	0x0A8	0.125	21	Example: DDR4-2133, 1 KB page size
120	0x078	0.125	15	Example: DDR4-2133, 1/2 KB page size
240	0x0F0	0.125	30	Example: DDR4-2400, 2 KB page size
168	0x0A8	0.125	21	Example: DDR4-2400, 1 KB page size
104	0x068	0.125	13	Example: DDR4-2400, 1/2 KB page size
		0.125	TBD	Example: DDR4-2666, 2 KB page size
		0.125	TBD	Example: DDR4-2666, 1 KB page size
		0.125	TBD	Example: DDR4-2666, 1/2 KB page size
		0.125	TBD	Example: DDR4-3200, 2 KB page size
		0.125	TBD	Example: DDR4-3200, 1 KB page size
		0.125	TBD	Example: DDR4-3200, 1/2 KB page size

Byte 38 (0x026): Minimum Activate to Activate Delay Time (t_{RRD_S}min), different bank group

This byte defines the minimum SDRAM Activate to Activate Delay Time to different bank groups in medium timebase (MTB) units. This value comes from the DDR4 SDRAM data sheet. Controller designers must also note that at some frequencies, a minimum number of clocks may be required resulting in a larger t_{RRD_S}min value than indicated in the SPD. For example, t_{RRD_S}min for DDR4-1600 must be 4 clocks.

Bits 7~0
Minimum Active to Active/Refresh Time (t_{RRD_S}min) MTB Units
Values defined from 1 to 255

If t_{RRD_S}min cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{RRD_S}min (SPD byte 119) used for correction to get the actual value.

Examples:

t_{RRD_S}min (MTB units)		MTB (ns)	t_{RRD_S}min Offset (FTB units)[1]		FTB (ns)	t_{RRD_S}min Result (ns)	Use
48	0x30	0.125	0	0	0.001	6.00	DDR4-1600 (800 MHz clock), 2 KB page size
40	0x28	0.125	0	0	0.001	5.00	DDR4-1600 (800 MHz clock), 1 KB page size
40	0x28	0.125	0	0	0.001	5.00	DDR4-1600 (800 MHz clock), 1/2 KB page size
43	0x2B	0.125	-76	0xB4	0.001	5.30	DDR4-1866 (933 MHz clock), 2 KB page size
34	0x22	0.125	-50	0xCE	0.001	4.20	DDR4-1866 (933 MHz clock), 1 KB page size
34	0x22	0.125	-50	0xCE	0.001	4.20	DDR4-1866 (933 MHz clock), 1/2 KB page size

t_{RRD_S}min (MTB units)		MTB (ns)	t_{RRD_S}min Offset (FTB units)[1]		FTB (ns)	t_{RRD_S}min Result (ns)	Use
43	0x2B	0.125	-76	0xB4	0.001	5.30	DDR4-2133 (1066 MHz clock), 2 KB page size
30	0x1E	0.125	-50	0xCE	0.001	3.70	DDR4-2133 (1066 MHz clock), 1 KB page size
30	0x1E	0.125	-50	0xCE	0.001	3.70	DDR4-2133 (1066 MHz clock), 1/2 KB page size
43	0x2B	0.125	-76	0xB4	0.001	5.30	DDR4-2400 (1200 MHz clock), 2 KB page size
27	0x1B	0.125	-76	0xB4	0.001	3.30	DDR4-2400 (1200 MHz clock), 1 KB page size
27	0x1B	0.125	-76	0xB4	0.001	3.30	DDR4-2400 (1200 MHz clock), 1/2 KB page size
		0.125			0.001	TBD	DDR4-2666 (1333 MHz clock)
		0.125			0.001	TBD	DDR4-3200 (1600 MHz clock)
Note 1 See SPD byte 119							

Byte 39 (0x027): Minimum Activate to Activate Delay Time (t_{RRD_L}min), same bank group

This byte defines the minimum SDRAM Activate to Activate Delay Time to the same bank group in medium timebase (MTB) units. This value comes from the DDR4 SDRAM data sheet. Controller designers must also note that at some frequencies, a minimum number of clocks may be required resulting in a larger t_{RRD_L}min value than indicated in the SPD. For example, t_{RRD_L}min for DDR4-1600 must be 4 clocks.

Bits 7~0
Minimum Active to Active/Refresh Time (t_{RRD_L}min) MTB Units
Values defined from 1 to 255

If t_{RRD_L}min cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{RRD_L}min (SPD byte 118) used for correction to get the actual value.

Examples:

t_{RRD_L}min (MTB units)		MTB (ns)	t_{RRD_L}min Offset (FTB units)[1]		FTB (ns)	t_{RRD_L}min Result (ns)	Use
60	0x3C	0.125	0	0	0.001	7.50	DDR4-1600 (800 MHz clock), 2 KB page size
48	0x30	0.125	0	0	0.001	6.00	DDR4-1600 (800 MHz clock), 1 KB page size
48	0x30	0.125	0	0	0.001	6.00	DDR4-1600 (800 MHz clock), 1/2 KB page size
52	0x34	0.125	-100	0x9C	0.001	6.40	DDR4-1866 (933 MHz clock), 2 KB page size
43	0x2B	0.125	-76	0xB4	0.001	5.30	DDR4-1866 (933 MHz clock), 1 KB page size
43	0x2B	0.125	-76	0xB4	0.001	5.30	DDR4-1866 (933 MHz clock), 1/2 KB page size
52	0x34	0.125	-100	0x9C	0.001	6.40	DDR4-2133 (1066 MHz clock), 2 KB page size
43	0x2B	0.125	-76	0xB4	0.001	5.30	DDR4-2133 (1066 MHz clock), 1 KB page size
43	0x2B	0.125	-76	0xB4	0.001	5.30	DDR4-2133 (1066 MHz clock), 1/2 KB page size
52	0x34	0.125	-100	0x9C	0.001	6.40	DDR4-2400 (1200 MHz clock), 2 KB page size
40	0x28	0.125	-100	0x9C	0.001	4.90	DDR4-2400 (1200 MHz clock), 1 KB page size
40	0x28	0.125	-100	0x9C	0.001	4.90	DDR4-2400 (1200 MHz clock), 1/2 KB page size
		0.125			0.001	TBD	DDR4-2666 (1333 MHz clock)
		0.125			0.001	TBD	DDR4-3200 (1600 MHz clock)
Note 1 See SPD byte 118							

Byte 40 (0x028): Minimum CAS to CAS Delay Time (t_{CCD_L}min), same bank group

This byte defines the minimum SDRAM CAS to CAS Delay Time to the same bank group in medium timebase (MTB) units. This value comes from the DDR4 SDRAM data sheet. Controller designers must also note that at some frequencies, a minimum number of clocks may be required resulting in a larger t_{CCD_L}min value than indicated in the SPD. For example, t_{CCD_L}min for DDR4-2133 must be 6 clocks.

Bits 7~0
Minimum CAS to CAS Time (t_{CCD_L}min) MTB Units
Values defined from 1 to 255

If t_{CCD_L}min cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{CCD_L}min (SPD byte 117) used for correction to get the actual value.

Examples:

t_{CCD_L}min (MTB units)		MTB (ns)	t_{CCD_L}min Offset (FTB units)[1]		FTB (ns)	t_{CCD_L} min Result (ns)	Use
50	0x32	0.125	0	0	0.001	6.250	DDR4-1600 (800 MHz clock)
43	0x2B	0.125	-20	0xEC	0.001	5.355	DDR4-1866 (933 MHz clock)
43	0x2B	0.125	-20	0xEC	0.001	5.355	DDR4-2133 (1066 MHz clock)
40	0x28	0.125	0	0	0.001	5.000	DDR4-2400 (1200 MHz clock)
		0.125			0.001	TBD	DDR4-2666 (1333 MHz clock)
		0.125			0.001	TBD	DDR4-3200 (1600 MHz clock)
Note 1 See SPD byte 117							

Byte 41~59 (0x029~0x03B): Reserved, Base Configuration Section

Must be coded as 0x00

Bytes 60~77 (0x03C~0x04D): Connector to SDRAM Bit Mapping

These bytes document the connection between data signals at the edge connector of a module to the DDR4 SDRAM inputs pins for package rank 0 of the module. This information is used by the controller to route data onto the correct bit lines for CRC transmission as described in the DDR4 SDRAM data sheet JESD79-4. Each byte describes the mapping for one nibble (four bits) of data. In addition, each SPD byte describes the mapping between package rank 0 bits and equivalent bits in other ranks.

SPD Byte		Connector Bits	SPD Byte		Connector Bits	SPD Byte		Connector Bits
60	0x03C	DQ0-3	66	0x042	DQ24-27	72	0x048	DQ40-43
61	0x03D	DQ4-7	67	0x043	DQ28-31	73	0x049	DQ44-47
62	0x03E	DQ8-11	68	0x044	CB0-3	74	0x04A	DQ48-51
63	0x03F	DQ12-15	69	0x045	CB4-7	75	0x04B	DQ52-55
64	0x040	DQ16-19	70	0x046	DQ32-35	76	0x04C	DQ56-59
65	0x041	DQ20-23	71	0x047	DQ36-39	77	0x04D	DQ60-63

The mapping rules are as follows:

- All bits within a nibble at the edge connector must be wired to the same SDRAM.
- All bits within a byte at the edge connector must be wired to the same SDRAM for x8 and wider SDRAMs.
- Bits within a nibble may be swapped in any order.
- Nibbles may be swapped within a byte.
- Bytes may be wired in any order within the SDRAM width for x16 and wider SDRAMs.

Each SPD byte in the Bit Mapping array is encoded as follows. If the nibble at the edge connector is wired to the lower nibble of a byte at the SDRAM (x8 and wider), then bit 5 is coded as 0. If the nibble at the edge connector is wired to the upper nibble of a byte at the SDRAM, then bit 5 is coded as 1. Bit 5 = 0 for all x4 based modules. Bits 6~7 define the connectivity between bits in different package ranks.

Bits 7 ~ 6	Bit 5	Bits 4 ~ 0
Package Rank Map	**Wired to Upper/Lower Nibble**	**Bit Order at SDRAM**
See Package Rank Map table	0 = lower nibble at SDRAM 1 = upper nibble at SDRAM	See Nibble Map table

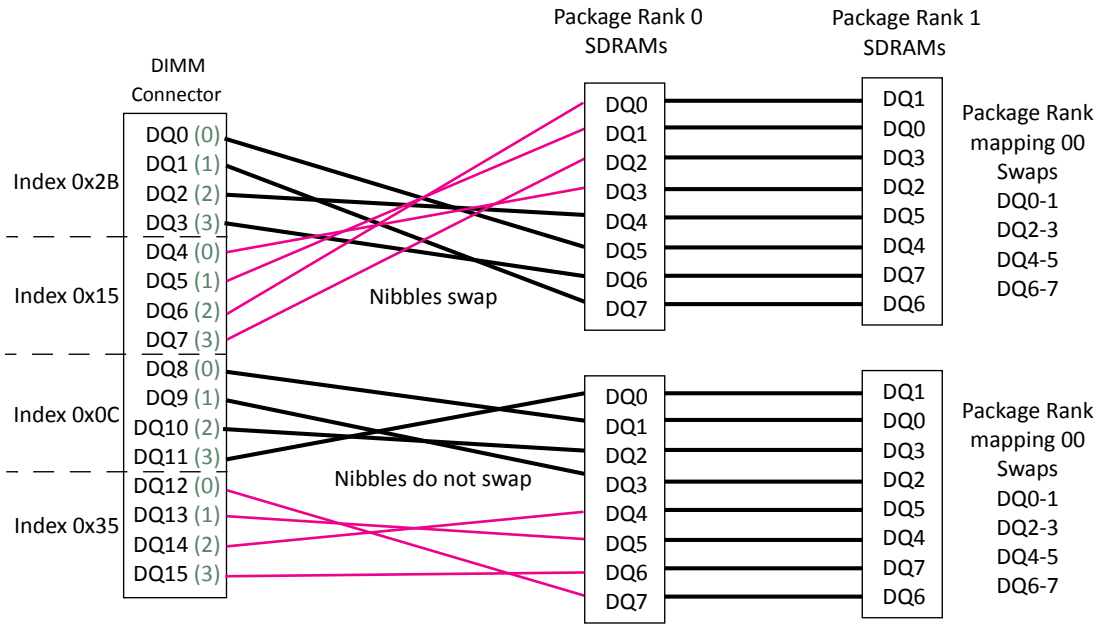
Package Rank Map: Bits 7~6 in each SPD byte define the mapping between bits in Package Rank 0 and other package ranks on the module. The mapping rules are defined in the following table:

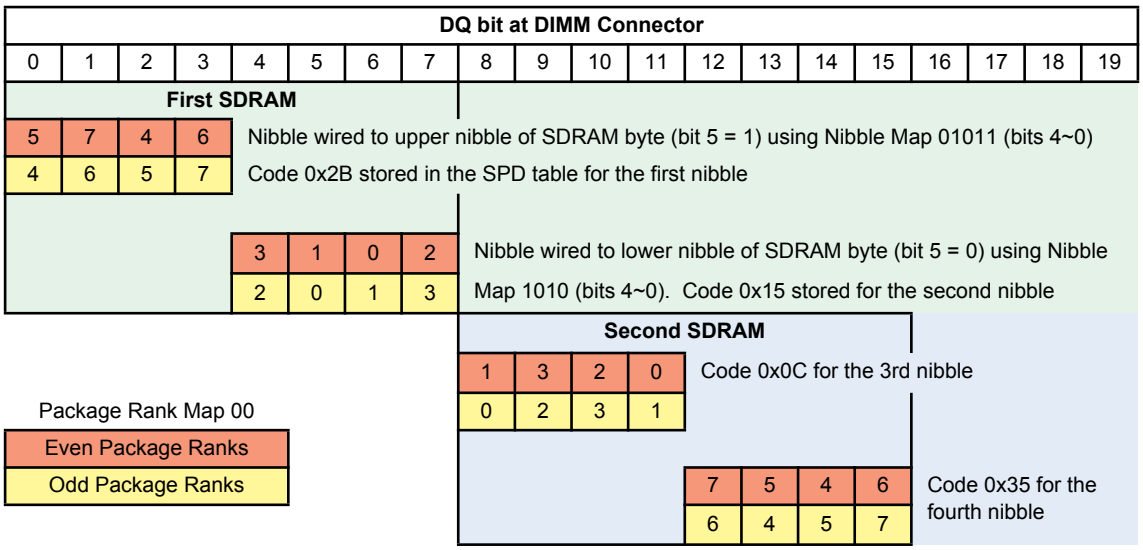
Package Rank Map				
Bits 7 ~ 6	**Bit Order at SDRAM**			
00	Even package ranks (0, 2, etc.) have the same mapping Odd package ranks (1, 3, etc) map SDRAM data bits relative to Package Rank 0 as follows:			
	DQ0 → DQ1	DQ8 → tbd	DQ16 → tbd	DQ24 → tbd
	DQ1 → DQ0	DQ9 → tbd	DQ17 → tbd	DQ25 → tbd
	DQ2 → DQ3	DQ10 → tbd	DQ18 → tbd	DQ26 → tbd
	DQ3 → DQ2	DQ11 → tbd	DQ19 → tbd	DQ27 → tbd
	DQ4 → DQ5	DQ12 → tbd	DQ20 → tbd	DQ28 → tbd
	DQ5 → DQ4	DQ13 → tbd	DQ21 → tbd	DQ29 → tbd
	DQ6 → DQ7	DQ14 → tbd	DQ22 → tbd	DQ30 → tbd
	DQ7 → DQ6	DQ15 → tbd	DQ23 → tbd	DQ31 → tbd
01 10 11	Reserved			

The Nibble Map is coded as follows:

Nibble Map					
Nibble Bit Order at Connector	**Bit Map Index Bits 4 ~ 0**	**Bit 5 = 0: Wired to Lower Nibble Bit Order within SDRAM Byte**		**Bit 5 = 1: Wired to Upper Nibble Bit Order within SDRAM Byte**	
	00000	0x00	Bit Map not specified	0x20	Bit Map not specified
0, 1, 2, 3 (4, 5, 6, 7) ...	00001	0x01	0, 1, 2, 3	0x21	4, 5, 6, 7
	00010	0x02	0, 1, 3, 2	0x22	4, 5, 7, 6
	00011	0x03	0, 2, 1, 3	0x23	4, 6, 5, 7
	00100	0x04	0, 2, 3, 1	0x24	4, 6, 7, 5
	00101	0x05	0, 3, 1, 2	0x25	4, 7, 5, 6
	00110	0x06	0, 3, 2, 1	0x26	4, 7, 6, 5
	00111	0x07	1, 0, 2, 3	0x27	5, 4, 6, 7
0, 1, 2, 3 (4, 5, 6, 7) ...	01000	0x08	1, 0, 3, 2	0x28	5, 4, 7, 6
	01001	0x09	1, 2, 0, 3	0x29	5, 6, 4, 7
	01010	0x0A	1, 2, 3, 0	0x2A	5, 6, 7, 4
	01011	0x0B	1, 3, 0, 2	0x2B	5, 7, 4, 6
	01100	0x0C	1, 3, 2, 0	0x2C	5, 7, 6, 4
	01101	0x0D	2, 0, 1, 3	0x2D	6, 4, 5, 7
	01110	0x0E	2, 0, 3, 1	0x2E	6, 4, 7, 5
	01111	0x0F	2, 1, 0, 3	0x2F	6, 5, 4, 7
0, 1, 2, 3 (4, 5, 6, 7) ...	10000	0x10	2, 1, 3, 0	0x30	6, 5, 7, 4
	10001	0x11	2, 3, 0, 1	0x31	6, 7, 4, 5
	10010	0x12	2, 3, 1, 0	0x32	6, 7, 5, 4
	10011	0x13	3, 0, 1, 2	0x33	7, 4, 5, 6
	10100	0x14	3, 0, 2, 1	0x34	7, 4, 6, 5
	10101	0x15	3, 1, 0, 2	0x35	7, 5, 4, 6
	10110	0x16	3, 1, 2, 0	0x36	7, 5, 6, 4
	10111	0x17	3, 2, 0, 1	0x37	7, 6, 4, 5
	11000	0x18	3, 2, 1, 0	0x38	7, 6, 5, 4
	All other codes		Reserved		Reserved
Note 1 Note: Hex codes shown in this table are for bits 5~0 only and must be added to bits 7~6 (Package Rank Map bits) for the SPD byte entry					

Example: Two Package Rank x8 Module (example only; may not represent a specific design)





Bytes 78~116 (0x04E~0x074): Reserved, Base Configuration Section

Must be coded as 0x00

Byte 117 (0x075): Fine Offset for Minimum CAS to CAS Delay Time (t_{CCD_L}min), same bank group

This byte modifies the calculation of SPD Byte 40 with a fine correction using FTB units. The value of t_{CCD_L}min comes from the SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 40. For Two's Complement encoding, see **Relating the MTB and FTB.**

Byte 118 (0x076): Fine Offset for Minimum Activate to Activate Delay Time (t_{RRD_L}min), same bank group

This byte modifies the calculation of SPD Byte 39 with a fine correction using FTB units. The value of t_{RRD_L}min comes from the SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 39. For Two's Complement encoding, see **Relating the MTB and FTB.**

Byte 119 (0x077): Fine Offset for Minimum Activate to Activate Delay Time (t_{RRD_S}min), different bank group

This byte modifies the calculation of SPD Byte 38 (MTB units) with a fine correction using FTB units. The value of t_{RRD_S}min comes from the SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 38. For Two's Complement encoding, see **Relating the MTB and FTB.**

Byte 120 (0x078): Fine Offset for Minimum Active to Active/Refresh Delay Time (t_{RC}min)

This byte modifies the calculation of SPD Bytes 27 and 29 (MTB units) with a fine correction using FTB units. The value of t_{RC}min comes from the SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD bytes 27 and 29. For Two's Complement encoding, see **Relating the MTB and FTB.**

Byte 121 (0x079): Fine Offset for Minimum Row Precharge Delay Time (t_{RP}min)

This byte modifies the calculation of SPD Byte 26 (MTB units) with a fine correction using FTB units. The value of t_{RP}min comes from the SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 26. For Two's Complement encoding, see **Relating the MTB and FTB.**

Byte 122 (0x07A): Fine Offset for Minimum RAS to CAS Delay Time (t_{RCD}min)

This byte modifies the calculation of SPD Byte 25 (MTB units) with a fine correction using FTB units. The value of t_{RCD}min comes from the SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 25. For Two's Complement encoding, see **Relating the MTB and FTB.**

Byte 123 (0x07B): Fine Offset for Minimum CAS Latency Time (t_{AA}min)

This byte modifies the calculation of SPD Byte 24 (MTB units) with a fine correction using FTB units. The value of t_{AA}min comes from the SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD Byte 24. For Two's Complement encoding, see **Relating the MTB and FTB.**

Byte 124 (0x07C): Fine Offset for SDRAM Maximum Cycle Time (t_{CKAVG}max)

This byte modifies the calculation of SPD Byte 19 (MTB units) with a fine correction using FTB units. The value of t_{CKAVG}max comes from the SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 19. For Two's Complement encoding, see **Relating the MTB and FTB.**

Byte 125 (0x07D): Fine Offset for SDRAM Minimum Cycle Time (t_{CKAVG}min)

This byte modifies the calculation of SPD Byte 18 (MTB units) with a fine correction using FTB units. The value of t_{CKAVG}min comes from the SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 18. For Two's Complement encoding, see **Relating the MTB and FTB.**

Byte 126 (0x07E): Cyclical Redundancy Code (CRC) for Base Configuration Section, LSB
Byte 127 (0x07F): Cyclical Redundancy Code (CRC) for Base Configuration Section, MSB

This two-byte field contains the calculated CRC for bytes 0~125 (0x000~0x07D) in the SPD. The following algorithm and data structures (shown in C) are to be followed in calculating and checking the code.

```
int Crc16 (char *ptr, int count)
{
   int crc, i;

   crc = 0;
   while (--count >= 0) {
      crc = crc ^ (int)*ptr++ << 8;
      for (i = 0; i < 8; ++i)
         if (crc & 0x8000)
            crc = crc << 1 ^ 0x1021;
         else
            crc = crc << 1;
   }
   return (crc & 0xFFFF);
}

char spdBytes[] = { SPD_byte_0, SPD_byte_1, ..., SPD_byte_N-1 };
int data16;

data16 = Crc16 (spdBytes, sizeof(spdBytes));
SPD_byte_126 = (char) (data16 & 0xFF);
SPD_byte_127 = (char) (data16 >> 8);
```

2.2 Module-Specific Sections: Bytes 128~255 (0x080~0x0FF)

The content of bytes 128~255 (0x080~0x0FF) of this SPD are determined according to specific DDR4 module families. Module Type Key Byte 3 is used as an index for the encoding of bytes 128~255.

At the end of this Annex there are separate subsections, one for each DDR4 module family, that define the bytes in SPD locations 128~255 (0x080~0x0FF). These module families and their respective subsections are:

- Annex L.1: Unbuffered Memory Modules
- Annex L.2: Registered Memory Modules
- Annex L.3: Load Reduced Memory Modules

2.3 Module Supplier's Data: Bytes 320~383 (0x140~0x17F)

Byte 320 (0x140): Module Manufacturer ID Code, LSB
Byte 321 (0x141): Module Manufacturer ID Code, MSB

This two-byte field indicates the manufacturer of the module, encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106.

Byte 321, Bits 7~0	Byte 320, Bit 7	Byte 320, Bits 6~0
Last non-zero byte, Module Manufacturer	**Odd Parity for Byte 320, bits 6~0**	**Number of continuation codes, Module Manufacturer**
See JEP-106		See JEP-106

Examples:

Company	JEP-106		# continuation codes	SPD	
	Bank	Code		Byte 320	Byte 321
Fujitsu	1	04	0	0x80	0x04
US Modular	5	A0	4	0x04	0xA8

Byte 322 (0x142): Module Manufacturing Location

The module manufacturer includes an identifier that uniquely defines the manufacturing location of the memory module. While the SPD specification will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

Bytes 323~324 (0x143~0x144): Module Manufacturing Date

The module manufacturer includes a date code for the module. The JEDEC definitions for bytes 323 and 324 are year and week respectively. These bytes must be represented in Binary Coded Decimal (BCD). For example, week 47 in year 2014 would be coded as 0x14 (0001 0100) in byte 323 and 0x47 (0100 0111) in byte 324.

Bytes 325~328 (0x145~0x148): Module Serial Number

The supplier must include a unique serial number for the module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

One method of achieving this is by assigning a byte in the field from 325~328 as a tester ID byte and using the remaining bytes as a sequential serial number. Bytes 320~328 will then result in a nine-byte unique module identifier. Note that part number is not included in this identifier: the supplier may not give the same value for Bytes 320~328 to more than one DIMM even if the DIMMs have different part numbers.

Bytes 329~348 (0x149~15C): Module Part Number

The manufacturer's part number is written in ASCII format within these bytes. Unused digits are coded as ASCII blanks (0x20).

Bytes 349 (0x15D): Module Revision Code

This refers to the module revision code. While the SPD specification will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte. This revision code refers to the manufacturer's assembly revision level and may be different than the raw card revision in SPD bytes 128 and 130.

Byte 350 (0x15E): DRAM Manufacturer ID Code, LSB
Byte 351 (0x15F): DRAM Manufacturer ID Code, MSB

This two-byte field indicates the manufacturer of the DRAM on the module, encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106.

Byte 351, Bits 7~0	Byte 350, Bit 7	Byte 350, Bits 6~0
Last non-zero byte, DRAM Manufacturer	**Odd Parity for Byte 350, bits 6~0**	**Number of continuation codes, DRAM Manufacturer**
See JEP-106		See JEP-106

Example: See bytes 320~321 for example manufacturer codes.

Byte 352 (0x160): DRAM Stepping

This byte defines the vendor die revision level (often called the “stepping”) of the DRAMs on the module. This byte is optional. For modules without DRAM stepping information, this byte should be programmed to 0xFF.

Bits 7~0
DRAM Stepping
Programmed in straight Hex format - no conversion needed. 00 - Valid 01 - Valid .. FE - Valid FF - Undefined (No Stepping Number Provided)

Examples:

Code	Meaning
0x00	Stepping 0
0x01	Stepping 1
0x31	Stepping 3.1
0xA3	Stepping A3
0xB1	Stepping B1
0xFF	Stepping information not provided

Bytes 353~381 (0x161~0x17D): Manufacturer’s Specific Data

The module manufacturer may include any additional information desired into the module within these locations.

Byte 382~383 (0x17E~0x17F): Reserved

ASCII Decode Matrix for SPDs

The following table is a subset of the full ASCII standard which is used for coding bytes in the Serial Presence Detect EEPROM that require ASCII characters:

	Second Hex Digit in Pair															
First Hex Digit in Pair	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
2	Blank Space								(	)				- Dash	. Period	
3	0	1	2	3	4	5	6	7	8	9						
4		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z					
6		a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z					

Examples:

0x20 = Blank Space
0x34 = ‘4’
0x41 = ‘A’

SPD Bytes 329~348	
Manufacturer’s PN	**Coded in ASCII**
13M32734BCD-260Y	31334D33323733344243442D323630592020

Annex L.1: Module Specific Bytes for Unbuffered Memory Module Types (Bytes 128~255, 0x080~0x0FF)

This section defines the encoding of SPD bytes 128~255 when Memory Technology Key Byte 2 contains the value 0x0C and Module Type Key Byte 3 contains any of the following:

- 0x02, UDIMM
- 0x03, SO-DIMM

The following is the SPD address map for the module specific section, bytes 128~255, of the SPD for Unbuffered Module Types.

Module Specific SPD Bytes for Unbuffered Module Types			
Byte Number		**Function Described**	**Notes**
128	0x080	Raw Card Extension, Module Nominal Height	
129	0x081	Module Maximum Thickness	
130	0x082	Reference Raw Card Used	
131	0x083	Address Mapping from Edge Connector to DRAM	
132~253	0x084~0x0FD	Reserved -- Must be coded as 0x00	
254	0x0FE	CRC for Module Specific Section, Least Significant Byte	
255	0x0FF	CRC for Module Specific Section, Most Significant Byte	

Byte 128 (0x080) (Unbuffered): Raw Card Extension, Module Nominal Height

The upper 3 bits of this byte define extensions to the Raw Card Revision in Byte 130. The lower 5 bits of this byte define the nominal height (A dimension) in millimeters of the fully assembled module including heat spreaders or other added components. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

Bits 7~5	**Bits 4~0**
Raw Card Extension	**Module Nominal Height max, in mm (baseline height = 15 mm)**
000 = raw card revisions 0 to 3; see byte 130 001 = raw card revision 4 010 = raw card revision 5 011 = raw card revision 6 100 = raw card revision 7 101 = raw card revision 8 110 = raw card revision 9 111 = raw card revision 10	00000 = height ≤ 15 mm 00001 = 15 < height ≤ 16 mm 00010 = 16 < height ≤ 17 mm 00011 = 17 < height ≤ 18 mm 00100 = 18 < height ≤ 19 mm ... 01010 = 24 < height ≤ 25 mm 01011 = 25 < height ≤ 26 mm ... 01111 = 29 < height ≤ 30 mm 10000 = 30 < height ≤ 31 mm 10001 = 31 < height ≤ 32 mm ... 11111 = 45 mm < height

Examples:

Nominal Module Height	Coding, bits 4~0	Meaning
mm	Binary	mm
18.75	00100	18 < height ≤ 19 mm
25.40	01011	25 < height ≤ 26 mm
30.00	01111	29 < height ≤ 30 mm
30.25	10000	30 < height ≤ 31 mm
31.25	10001	30 < height ≤ 31 mm

Byte 129 (0x081) (Unbuffered): Module Maximum Thickness

This byte defines the maximum thickness (E dimension) in millimeters of the fully assembled module including heat spreaders or other added components above the module circuit board surface. Thickness of the front of the module is calculated as the E1 dimension minus the PCB thickness. Thickness of the back of the module is calculated as the E dimension minus the E1 dimension, rounding up to the next integer. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

Bits 7~4	Bits 3~0
Module Maximum Thickness max, Back, in mm (baseline thickness = 1 mm)	**Module Maximum Thickness max, Front, in mm (baseline thickness = 1 mm)**
0000 = thickness ≤ 1 mm 0001 = 1 < thickness ≤ 2 mm 0010 = 2 < thickness ≤ 3 mm 0011 = 3 < thickness ≤ 4 mm ... 1110 = 14 < thickness ≤ 15 mm 1111 = 15 < thickness	0000 = thickness ≤ 1 mm 0001 = 1 < thickness ≤ 2 mm 0010 = 2 < thickness ≤ 3 mm 0011 = 3 < thickness ≤ 4 mm ... 1110 = 14 < thickness ≤ 15 mm 1111 = 15 < thickness
Note 1 Thickness = E - E1	**Note 2** Thickness = E1 - PCB

Byte 130 (0x082) (Unbuffered): Reference Raw Card Used

This byte indicates which JEDEC reference design raw card was used as the basis for the module assembly, if any. Bits 4~0 describe the raw card and bits 6~5 describe the revision level of that raw card. Special reference raw card indicator, ZZ, is used when no JEDEC standard raw card reference design was used as the basis for the module design. Pre-production modules should be encoded as revision 0 in bits 6~5.

Bit 7	Bits 6~5	Bits 4~0
Reference Raw Card Extension	**Reference Raw Card Revision**	**Reference Raw Card**
0 = Reference raw cards A through AL	00 = revision 0 01 = revision 1 10 = revision 2 11 = revision 3 See byte 128 for extensions beyond revision 3; these bits must be coded as 11 for all revisions greater than 3	When bit 7 = 0, 00000 = Reference raw card A 00001 = Reference raw card B 00010 = Reference raw card C 00011 = Reference raw card D 00100 = Reference raw card E 00101 = Reference raw card F 00110 = Reference raw card G 00111 = Reference raw card H 01000 = Reference raw card J 01001 = Reference raw card K 01010 = Reference raw card L 01011 = Reference raw card M 01100 = Reference raw card N 01101 = Reference raw card P 01110 = Reference raw card R 01111 = Reference raw card T 10000 = Reference raw card U 10001 = Reference raw card V 10010 = Reference raw card W 10011 = Reference raw card Y 10100 = Reference raw card AA 10101 = Reference raw card AB 10110 = Reference raw card AC 10111 = Reference raw card AD 11000 = Reference raw card AE 11001 = Reference raw card AF 11010 = Reference raw card AG 11011 = Reference raw card AH 11100 = Reference raw card AJ 11101 = Reference raw card AK 11110 = Reference raw card AL 11111 = ZZ (no JEDEC reference raw card design used)

Bit 7	Bits 6~5	Bits 4~0
Reference Raw Card Extension	**Reference Raw Card Revision**	**Reference Raw Card**
1 = Reference raw cards AM through CB	00 = revision 0 01 = revision 1 10 = revision 2 11 = revision 3 See byte 128 for extensions beyond revision 3; these bits must be coded as 11 for all revisions greater than 3	When bit 7 = 1, 00000 = Reference raw card AM 00001 = Reference raw card AN 00010 = Reference raw card AP 00011 = Reference raw card AR 00100 = Reference raw card AT 00101 = Reference raw card AU 00110 = Reference raw card AV 00111 = Reference raw card AW 01000 = Reference raw card AY 01001 = Reference raw card BA 01010 = Reference raw card BB 01011 = Reference raw card BC 01100 = Reference raw card BD 01101 = Reference raw card BE 01110 = Reference raw card BF 01111 = Reference raw card BG 10000 = Reference raw card BH 10001 = Reference raw card BJ 10010 = Reference raw card BK 10011 = Reference raw card BL 10100 = Reference raw card BM 10101 = Reference raw card BN 10110 = Reference raw card BP 10111 = Reference raw card BR 11000 = Reference raw card BT 11001 = Reference raw card BU 11010 = Reference raw card BV 11011 = Reference raw card BW 11100 = Reference raw card BY 11101 = Reference raw card CA 11110 = Reference raw card CB 11111 = ZZ (no JEDEC reference raw card design used)

Byte 131 (0x083) (Unbuffered): Address Mapping from Edge Connector to DRAM

This byte describes the connection of edge connector pins for address bits to the corresponding input pins of the DDR4 SDRAMs for rank 1 only; rank 0 is always assumed to use standard mapping. Only two connection types are supported, standard or mirrored, as described in the mapping table below. System software must compensate for this mapping when issuing mode register set commands to the ranks of DDR4 SDRAMs on this module.

Bits 7~1	Bit 0
Reserved	**Rank 1 Mapping**
Reserved	0 = standard 1 = mirrored

The definition of standard and mirrored address connection mapping is detailed below; highlighted rows in the table indicate which signals change between mappings.

Edge Connector Pin	DRAM Pin, Non-mirrored	DRAM Pin, Mirrored
A0	A0	A0
A1	A1	A1
A2	A2	A2
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
A9	A9	A9
A10	A10	A10
A11	A11	A13
A13	A13	A11
A12	A12	A12
A14	A14	A14
A15	A15	A15
A16	A16	A16
A17	A17	A17
BA0	BA0	BA1
BA1	BA1	BA0
BG0	BG0	BG1
BG1	BG1	BG0

Bytes 132~253 (0x084~0x0FD) (Unbuffered):

Reserved -- must be coded as 0x00

Byte 254 (0x0FE) (Unbuffered): Cyclical Redundancy Code (CRC) for Module Specific Section, LSB

Byte 255 (0x0FF) (Unbuffered): Cyclical Redundancy Code (CRC) for Module Specific Section, MSB

This two-byte field contains the calculated CRC for bytes 128~253 (0x080~0x0FD) in the SPD. See bytes 126~127 for a coding example.

Annex L.2: Module Specific Bytes for Registered Memory Module Types (Bytes 128~255, 0x080~0x0FF)

This section defines the encoding of SPD bytes 128~255 when Memory Technology Key Byte 2 contains the value 0x0C and Module Type Key Byte 3 contains any of the following:

- 0x01, RDIMM

The following is the SPD address map for the module specific section, bytes 128~255, of the SPD for Registered Module Types.

Module Specific SPD Bytes for Registered Module Types			
Byte Number		Function Described	Notes
128	0x080	Raw Card Extension, Module Nominal Height	
129	0x081	Module Maximum Thickness	
130	0x082	Reference Raw Card Used	
131	0x083	DIMM Module Attributes	
132	0x084	RDIMM Thermal Heat Spreader Solution	
133	0x085	Register Manufacturer ID Code, Least Significant Byte	
134	0x086	Register Manufacturer ID Code, Most Significant Byte	
135	0x087	Register Revision Number	
136	0x088	Address Mapping from Register to DRAM	
137~253	0x089~0x0FD	Reserved -- must be coded as 0x00	
254	0x0FE	CRC for Module Specific Section, Least Significant Byte	
255	0x0FF	CRC for Module Specific Section, Most Significant Byte	

Byte 128 (0x080) (Registered): Raw Card Extension, Module Nominal Height

The upper 3 bits of this byte define extensions to the Raw Card Revision in Byte 130. The lower 5 bits of this byte define the nominal height (A dimension) in millimeters of the fully assembled module including heat spreaders or other added components. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

Bits 7~5	Bits 4~0
Raw Card Extension	**Module Nominal Height max, in mm (baseline height = 15 mm)**
000 = raw card revisions 0 to 3; see byte 130 001 = raw card revision 4 010 = raw card revision 5 011 = raw card revision 6 100 = raw card revision 7 101 = raw card revision 8 110 = raw card revision 9 111 = raw card revision 10	00000 = height ≤ 15 mm 00001 = 15 < height ≤ 16 mm 00010 = 16 < height ≤ 17 mm 00011 = 17 < height ≤ 18 mm 00100 = 18 < height ≤ 19 mm ... 01010 = 24 < height ≤ 25 mm 01011 = 25 < height ≤ 26 mm ... 01111 = 29 < height ≤ 30 mm 10000 = 30 < height ≤ 31 mm 10001 = 31 < height ≤ 32 mm ... 11111 = 45 mm < height

Examples:

Nominal Module Height	Coding, bits 4~0	Meaning
mm	Binary	mm
18.75	00100	18 < height ≤ 19 mm
25.40	01011	25 < height ≤ 26 mm
30.00	01111	29 < height ≤ 30 mm
30.25	10000	30 < height ≤ 31 mm
31.25	10001	31 < height ≤ 32 mm

Byte 129 (0x081) (Registered): Module Maximum Thickness

This byte defines the maximum thickness (E dimension) in millimeters of the fully assembled module including heat spreaders or other added components above the module circuit board surface, rounding up to the next integer. Thickness of the front of the module is calculated as the E1 dimension minus the PCB thickness. Thickness of the back of the module is calculated as the E dimension minus the E1 dimension. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

Bits 7~4	Bits 3~0
Module Maximum Thickness max, Back, in mm (baseline thickness = 1 mm)	**Module Maximum Thickness max, Front, in mm (baseline thickness = 1 mm)**
0000 = thickness ≤ 1 mm 0001 = 1 < thickness ≤ 2 mm 0010 = 2 < thickness ≤ 3 mm 0011 = 3 < thickness ≤ 4 mm ... 1110 = 14 < thickness ≤ 15 mm 1111 = 15 < thickness	0000 = thickness ≤ 1 mm 0001 = 1 < thickness ≤ 2 mm 0010 = 2 < thickness ≤ 3 mm 0011 = 3 < thickness ≤ 4 mm ... 1110 = 14 < thickness ≤ 15 mm 1111 = 15 < thickness
Note 1 Thickness = E - E1	**Note 2** Thickness = E1 - PCB

Byte 130 (0x082) (Registered): Reference Raw Card Used

This byte indicates which JEDEC reference design raw card was used as the basis for the module assembly, if any. Bits 4~0 describe the raw card and bits 6~5 describe the revision level of that raw card. Special raw card indicator, ZZ, is used when no JEDEC standard raw card was used as the basis for the design. Pre-production modules should be encoded as revision 0 in bits 6~5.

Bit 7	Bits 6~5	Bits 4~0
Reference Raw Card Extension	**Reference Raw Card Revision**	**Reference Raw Card**
0 = Reference raw cards A through AL	00 = revision 0 01 = revision 1 10 = revision 2 11 = revision 3 See byte 128 for extensions beyond revision 3; these bits must be coded as 11 for all revisions greater than 3	When bit 7 = 0, 00000 = Reference raw card A 00001 = Reference raw card B 00010 = Reference raw card C 00011 = Reference raw card D 00100 = Reference raw card E 00101 = Reference raw card F 00110 = Reference raw card G 00111 = Reference raw card H 01000 = Reference raw card J 01001 = Reference raw card K 01010 = Reference raw card L 01011 = Reference raw card M 01100 = Reference raw card N 01101 = Reference raw card P 01110 = Reference raw card R 01111 = Reference raw card T 10000 = Reference raw card U 10001 = Reference raw card V 10010 = Reference raw card W 10011 = Reference raw card Y 10100 = Reference raw card AA 10101 = Reference raw card AB 10110 = Reference raw card AC 10111 = Reference raw card AD 11000 = Reference raw card AE 11001 = Reference raw card AF 11010 = Reference raw card AG 11011 = Reference raw card AH 11100 = Reference raw card AJ 11101 = Reference raw card AK 11110 = Reference raw card AL 11111 = ZZ (no JEDEC reference raw card design used)

Bit 7	Bits 6~5	Bits 4~0
Reference Raw Card Extension	**Reference Raw Card Revision**	**Reference Raw Card**
1 = Reference raw cards AM through CB	00 = revision 0 01 = revision 1 10 = revision 2 11 = revision 3 See byte 128 for extensions beyond revision 3; these bits must be coded as 11 for all revisions greater than 3	When bit 7 = 1, 00000 = Reference raw card AM 00001 = Reference raw card AN 00010 = Reference raw card AP 00011 = Reference raw card AR 00100 = Reference raw card AT 00101 = Reference raw card AU 00110 = Reference raw card AV 00111 = Reference raw card AW 01000 = Reference raw card AY 01001 = Reference raw card BA 01010 = Reference raw card BB 01011 = Reference raw card BC 01100 = Reference raw card BD 01101 = Reference raw card BE 01110 = Reference raw card BF 01111 = Reference raw card BG 10000 = Reference raw card BH 10001 = Reference raw card BJ 10010 = Reference raw card BK 10011 = Reference raw card BL 10100 = Reference raw card BM 10101 = Reference raw card BN 10110 = Reference raw card BP 10111 = Reference raw card BR 11000 = Reference raw card BT 11001 = Reference raw card BU 11010 = Reference raw card BV 11011 = Reference raw card BW 11100 = Reference raw card BY 11101 = Reference raw card CA 11110 = Reference raw card CB 11111 = ZZ (no JEDEC reference raw card design used)

Byte 131 (0x083) (Registered): DIMM Module Attributes

This byte indicates number of registers used on a module. Further it indicates number of rows of DRAM packages (monolithic, DDP or other stacked) parallel to edge connector (independent of DRAM orientation) on each side of the printed circuit board.

Bit 7~Bit 4	Bit 3~Bit 2	Bit 1~Bit 0
Reserved	# of rows of DRAMs on RDIMM	# of Registers used on RDIMM
Reserved	00 = undefined 01 = 1 row 10 = 2 rows 11 = 4 rows	00 = Undefined 01 = 1 register 10 = 2 registers 11 = 4 registers

Examples: TBD

Byte 132 (0x084) (Registered): RDIMM Thermal Heat Spreader Solution

This byte describes the module's supported thermal heat spreader solution.

Bit 7	Bits 6~0
Heat Spreader Solution	**Heat Spreader Thermal Characteristics**
0 = Heat spreader solution is not incorporated onto this assembly 1 = Heat spreader solution is incorporated onto this assembly	0 = Undefined All other settings to be defined

Byte 133 (0x085) (Registered): Register Manufacturer ID Code, LSB
Byte 134 (0x086) (Registered): Register Manufacturer ID Code, MSB

This two-byte field indicates the manufacturer of the register used on the module, encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106. These bytes are optional. For modules without the Register Manufacturer ID Code information both bytes should be programmed to 0x00.

Byte 134, Bits 7~0	Byte 133, Bit 7	Byte 133 Bits 6~0
Last non-zero byte, Register Manufacturer	**Odd parity for Byte 133, bits 6~0**	**Number of continuation codes, Register Manufacturer**
See JEP-106		See JEP-106

Example: See SPD bytes 320~321 for example manufacturer codes.

Byte 135 (0x087) (Registered): Register Revision Number

This byte defines the vendor die revision level of the registering clock driver component. This byte is optional. For modules without the Register Revision Number information, this byte should be programmed to 0xFF.

Bits 7~0
Register Revision Number
Programmed in straight Hex format - no conversion needed. 00 - Valid 01 - Valid ... FE - Valid FF - Undefined (No Revision Number Provided)

Examples:

Code	Meaning
0x00	Revision 0
0x01	Revision 1
0x31	Revision 3.1
0xA3	Revision A3
0xB1	Revision B1

Code	Meaning
0xFF	Revision information not supplied

Byte 136 (0x088) (Registered): Address Mapping from Register to DRAM

This byte describes the connection of register output pins for address bits to the corresponding input pins of the DDR4 SDRAMs for rank 1 and rank 3 only; rank 0 and rank 2 are always assumed to use standard mapping. Only two connection types are supported, standard or mirrored, as described in the mapping table below. System software must compensate for this mapping when issuing mode register set commands to the ranks of DDR4 SDRAMs on this module.

Bits 7~1	Bit 0
Reserved	**Rank 1 Mapping**
Reserved	0 = standard 1 = mirrored

The definition of standard and mirrored address connection mapping is detailed below; highlighted rows in the table indicate which signals change between mappings.

Edge Connector Pin	DRAM Pin, Non-mirrored	DRAM Pin, Mirrored
A0	A0	A0
A1	A1	A1
A2	A2	A2
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
A9	A9	A9
A10	A10	A10
A11	A11	A13
A13	A13	A11
A12	A12	A12
A14	A14	A14
A15	A15	A15
A16	A16	A16
A17	A17	A17
BA0	BA0	BA1
BA1	BA1	BA0
BG0	BG0	BG1
BG1	BG1	BG0

Byte 137 (0x089) (Registered): Register Output Drive Strength for Control

This byte defines the drive strength for the registering clock driver outputs.

Register Output Drive Strength, Control							
Chip Select		Command/Address		ODT		CKE	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved		00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Very Strong Drive		00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved		00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved	
Note 1 Standard values for drive strength are defined in the DDR4 Registered DIMM Reference Design Specification for JEDEC standard module reference designs.							

Byte 138 (0x08A) (Registered): Register Output Drive Strength for CK

This byte defines the drive strength for the registering clock driver outputs.

Register Output Drive Strength, Clock							
Reserved				Y1, Y3		Y0, Y2	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved		00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved	
Note 1 Standard values for drive strength are defined in the DDR4 Registered DIMM Reference Design Specification for JEDEC standard module reference designs.							

Bytes 139~253 (0x08B~0x0FD) (Registered):

Reserved -- must be coded as 0x00

Byte 254 (0x0FE) (Registered): Cyclical Redundancy Code (CRC) for Module Specific Section, LSB

Byte 255 (0x0FF) (Registered): Cyclical Redundancy Code (CRC) for Module Specific Section, MSB

This two-byte field contains the calculated CRC for bytes 128~253 (0x080~0x0FD) in the SPD. See bytes 126~127 for a coding example.

Annex L.3: Module Specific Bytes for Load Reduction Memory Module Types (Bytes 128~255, 0x080~0x0FF)

This section defines the encoding of SPD bytes 128~255 when Memory Technology Key Byte 2 contains the value 0x0C and Module Type Key Byte 3 contains any of the following:

- 0x04, LRDIMM

The following is the SPD address map for the module specific section, bytes 128~ 255, of the SPD for Load Reduced Module Types.

Module Specific SPD Bytes for Load Reduced Module Types			
Byte Number		Function Described	Notes
128	0x080	Raw Card Extension, Module Nominal Height	
129	0x081	Module Maximum Thickness	
130	0x082	Reference Raw Card Used	
131	0x083	DIMM Module Attributes	
132	0x084	LRDIMM Thermal Heat Spreader Solution	
133	0x085	Register and Data Buffer Manufacturer ID Code, Least Significant Byte	
134	0x086	Register and Data Buffer Manufacturer ID Code, Most Significant Byte	
135	0x087	Register Revision Number	
136	0x088	Address Mapping from Register to DRAM	
137	0x089	Register Output Drive Strength for Control and Command/Address	
138	0x08A	Register Output Drive Strength for CK	
139	0x08B	Data Buffer Revision Number	
140	0x08C	DRAM VrefDQ for Package Rank 0	
141	0x08D	DRAM VrefDQ for Package Rank 1	
142	0x08E	DRAM VrefDQ for Package Rank 2	
143	0x08F	DRAM VrefDQ for Package Rank 3	
144	0x090	Data Buffer VrefDQ for DRAM Interface	
145	0x091	Data Buffer MDQ Drive Strength and RTT for data rate $\leq$ 1866	
146	0x092	Data Buffer MDQ Drive Strength and RTT for 1866 < data rate $\leq$ 2400	
147	0x093	Data Buffer MDQ Drive Strength and RTT for 2400 < data rate $\leq$ 3200	
148	0x094	DRAM Drive Strength (for data rates $\leq$ 1866, 1866 < data rate < 2400, and 2400 < data rate $\leq$ 3200)	
149	0x095	DRAM ODT (RTT_WR, RTT_NOM) for data rate $\leq$ 1866	
150	0x096	DRAM ODT (RTT_WR, RTT_NOM) for 1866 < data rate $\leq$ 2400	
151	0x097	DRAM ODT (RTT_WR, RTT_NOM) for 2400 < data rate $\leq$ 3200	
152	0x098	DRAM ODT (RTT_PARK) for data rate $\leq$ 1866	
153	0x099	DRAM ODT (RTT_PARK) for 1866 < data rate $\leq$ 2400	
154	0x09A	DRAM ODT (RTT_PARK) for 2400 < data rate $\leq$ 3200	
155~253	0x09B~0x0FD	Reserved -- must be coded as 0x00	
254	0x0FE	CRC for Module Specific Section, Least Significant Byte	
255	0x0FF	CRC for Module Specific Section, Least Significant Byte	

Byte 128 (0x080) (Load Reduced): Raw Card Extension, Module Nominal Height

The upper 3 bits of this byte define extensions to the Raw Card Revision in Byte 130. The lower 5 bits of this byte define the nominal height (A dimension) in millimeters of the fully assembled module including heat spreaders or other added components. Refer to the relevant JEDEC JC-11 module outline (MO309A) documents for dimension definitions.

Bits 7 ~ 5	Bits 4 ~ 0
Raw Card Extension	**Module Nominal Height max, in mm (baseline height = 15 mm)**
000 = raw card revisions 0 to 3; see byte 130 001 = raw card revision 4 010 = raw card revision 5 011 = raw card revision 6 100 = raw card revision 7 101 = raw card revision 8 110 = raw card revision 9 111 = raw card revision 10	00000 = height ≤ 15 mm 00001 = 15 < height ≤ 16 mm 00010 = 16 < height ≤ 17 mm 00011 = 17 < height ≤ 18 mm 00100 = 18 < height ≤ 19 mm ... 01010 = 24 < height ≤ 25 mm 01011 = 25 < height ≤ 26 mm ... 01111 = 29 < height ≤ 30 mm 10000 = 30 < height ≤ 31 mm ... 11111 = 45 mm < height

Examples:

Nominal Module Height	Coding, bits 4 ~ 0	Meaning
mm	Binary	mm
18.75	00100	18 < height ≤ 19 mm
25.40	01011	25 < height ≤ 26 mm
30.00	01111	29 < height ≤ 30 mm
30.25	10000	30 < height ≤ 31 mm
31.25	10001	31 < height ≤ 32 mm

Byte 129 (0x081) (Load Reduced): Module Maximum Thickness

This byte defines the maximum thickness (E dimension) in millimeters of the fully assembled module including heat spreaders or other added components above the module circuit board surface, rounding up to the next integer. Thickness of the front of the module is calculated as the E1 dimension minus the PCB thickness. Thickness of the back of the module is calculated as the E dimension minus the E1 dimension. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

Bits 7 ~ 4	Bits 3 ~ 0
Module Maximum Thickness max, Back, in mm (baseline thickness = 1 mm)	**Module Maximum Thickness max, Front, in mm (baseline thickness = 1 mm)**
0000 = thickness ≤ 1 mm 0001 = 1 < thickness ≤ 2 mm 0010 = 2 < thickness ≤ 3 mm 0011 = 3 < thickness ≤ 4 mm ... 1110 = 14 < thickness ≤ 15 mm 1111 = 15 < thickness	0000 = thickness ≤ 1 mm 0001 = 1 < thickness ≤ 2 mm 0010 = 2 < thickness ≤ 3 mm 0011 = 3 < thickness ≤ 4 mm ... 1110 = 14 < thickness ≤ 15 mm 1111 = 15 < thickness
Note 1 Thickness = E - E1	**Note 2** Thickness = E1 - PCB

Byte 130 (0x082) (Load Reduced): Reference Raw Card Used

This byte indicates which JEDEC reference design raw card was used as the basis for the module assembly, if any. Bits 4~0 describe the raw card and bits 6~5 describe the revision level of that raw card. Special raw card indicator, ZZ, is used when no JEDEC standard raw card was used as the basis for the design. Pre-production modules should be encoded as revision 0 in bits 6~5.

Bit 7	Bits 6 ~ 5	Bits 4 ~ 0
Reference Raw Card Extension	**Reference Raw Card Revision**	**Reference Raw Card**
0 = Reference raw cards A through AL	00 = revision 0 01 = revision 1 10 = revision 2 11 = revision 3 See byte 128 for extensions beyond revision 3; these bits must be coded as 11 for all revisions greater than 3	When bit 7 = 0, 00000 = Reference raw card A 00001 = Reference raw card B 00010 = Reference raw card C 00011 = Reference raw card D 00100 = Reference raw card E 00101 = Reference raw card F 00110 = Reference raw card G 00111 = Reference raw card H 01000 = Reference raw card J 01001 = Reference raw card K 01010 = Reference raw card L 01011 = Reference raw card M 01100 = Reference raw card N 01101 = Reference raw card P 01110 = Reference raw card R 01111 = Reference raw card T 10000 = Reference raw card U 10001 = Reference raw card V 10010 = Reference raw card W 10011 = Reference raw card Y 10100 = Reference raw card AA 10101 = Reference raw card AB 10110 = Reference raw card AC 10111 = Reference raw card AD 11000 = Reference raw card AE 11001 = Reference raw card AF 11010 = Reference raw card AG 11011 = Reference raw card AH 11100 = Reference raw card AJ 11101 = Reference raw card AK 11110 = Reference raw card AL 11111 = ZZ (no JEDEC reference raw card design used)

Bit 7	Bits 6 ~ 5	Bits 4 ~ 0
Reference Raw Card Extension	**Reference Raw Card Revision**	**Reference Raw Card**
1 = Reference raw cards AM through CB	00 = revision 0 01 = revision 1 10 = revision 2 11 = revision 3 See byte 128 for extensions beyond revision 3; these bits must be coded as 11 for all revisions greater than 3	When bit 7 = 1, 00000 = Reference raw card AM 00001 = Reference raw card AN 00010 = Reference raw card AP 00011 = Reference raw card AR 00100 = Reference raw card AT 00101 = Reference raw card AU 00110 = Reference raw card AV 00111 = Reference raw card AW 01000 = Reference raw card AY 01001 = Reference raw card BA 01010 = Reference raw card BB 01011 = Reference raw card BC 01100 = Reference raw card BD 01101 = Reference raw card BE 01110 = Reference raw card BF 01111 = Reference raw card BG 10000 = Reference raw card BH 10001 = Reference raw card BJ 10010 = Reference raw card BK 10011 = Reference raw card BL 10100 = Reference raw card BM 10101 = Reference raw card BN 10110 = Reference raw card BP 10111 = Reference raw card BR 11000 = Reference raw card BT 11001 = Reference raw card BU 11010 = Reference raw card BV 11011 = Reference raw card BW 11100 = Reference raw card BY 11101 = Reference raw card CA 11110 = Reference raw card CB 11111 = ZZ (no JEDEC reference raw card design used)

Byte 131 (0x083) (Load Reduced): DIMM Module Attributes

This byte indicates number of registers used on a module. Further it indicates number of rows of DRAM packages (monolithic, DDP or 3D stacked) parallel to edge connector (independent of DRAM orientation) on each side of the printed circuit board.

Bits 7~4	Bits 3~2	Bits 1~0
Reserved	**# of rows of DRAMs on LRDIMM**	**# of Registers used on LRDIMM**
Reserved	00 = Undefined 01 = 1 row 10 = 2 rows 11 = undefined	00 = Undefined 01 = 1 register 10 = Reserved 11 = Reserved

Examples: TBD

Byte 132 (0x084) (Load Reduced): LRDIMM Thermal Heat Spreader Solution

This byte describes if the module assembly incorporates a heat spreader.

Bit 7	Bit 6~0
Heat Spreader	**Heat Spreader Thermal Characteristics**
0 = Heat spreader solution is not incorporated onto this assembly 1 = Heat spreader solution is incorporated onto this assembly	Undefined

Byte 133 (0x085) (Load Reduced): Register and Data Buffer Manufacturer ID Code, LSB

Byte 134 (0x086) (Load Reduced): Register and Data Buffer Manufacturer ID Code, MSB

This two-byte field indicates the manufacturer of the memory buffer used on the module, encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106.

Byte tbd, Bits 7 ~ 0	Byte tbd, Bit 7	Byte tbd Bits 6 ~ 0
Last non-zero byte, Memory Buffer Manufacturer	**Odd parity for Byte 133, bits 6 ~ 0**	**Number of continuation codes, Memory Buffer Manufacturer**
See JEP-106		See JEP-106

Example: See SPD byte 320~321 for example manufacturer codes.

Byte 135 (0x087) (Load Reduced): Register Revision Number

This byte defines the vendor die revision level of the registering clock driver component.

Bits 7 ~ 0
Register Revision Number
Programmed in straight Hex format - no conversion needed. 00 - Valid 01 - Valid .. FE - Valid FF - Undefined

Examples:

Code	Meaning
0x00	Revision 0
0x01	Revision 1
0x31	Revision 3.1
0xA3	Revision A3
0xB1	Revision B1

Byte 136 (0x088) (Load Reduced): Address Mapping from Register to DRAM

This byte describes the connection of register output pins for address bits to the corresponding input pins of the DDR4 SDRAMs for odd ranks only; even ranks are always assumed to use standard mapping. Only two connection types are currently supported, all rank non-mirrored or odd ranks mirrored, as described in the mapping table below. System software must compensate for this mapping when issuing mode register set commands to the ranks of DDR4 SDRAMs on this module.

Bits 7 ~ 1	Bits 0
Reserved	**Odd Rank Mapping**
Reserved	0 = standard 1 = mirrored

The definition of standard and mirrored address connection mapping is detailed below; highlighted rows in the table indicate which signals change between mappings.

Edge Connector Pin	DRAM Pin, Non-mirrored	DRAM Pin, Mirrored
A0	A0	A0
A1	A1	A1
A2	A2	A2
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
A9	A9	A9
A10	A10	A10
A11	A11	A13
A13	A13	A11
A12	A12	A12
A14	A14	A14
A15	A15	A15
A16	A16	A16
A17	A17	A17
BA0	BA0	BA1
BA1	BA1	BA0
BG0	BG0	BG1
BG1	BG1	BG0

Byte 137 (0x089) (Load Reduced): Register Output Drive Strength for Control and Command/ Address

This byte defines the drive strength for control and command/address outputs of the registering clock driver component.

Register Output Drive Strength for Control and Command/Address							
Chip Select		Command/Address		ODT		CKE	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved		00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Very Strong Drive		00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved		00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved	
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Specification for JEDEC standard module reference designs.							

Byte 138 (0x08A) (Load Reduced): Register Output Drive Strength for CK

This byte defines the drive strength for clock outputs of the registering clock driver component.

Register Output Drive Strength for CK							
Reserved				Y1, Y3		Y0, Y2	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved		00 = Light Drive 01 = Moderate Drive 10 = Strong Drive 11 = Reserved	
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Byte 139 (0x08B) (Load Reduced): Data Buffer Revision Number

This byte defines the vendor die revision level of the data buffer component.

Bits 7 ~ 0
Data Buffer Revision Number
Programmed in straight Hex format - no conversion needed. 00 - Valid 01 - Valid .. FE - Valid FF - Undefined

Examples:

Code	Meaning
0x00	Revision 0
0x01	Revision 1
0x31	Revision 3.1
0xA3	Revision A3
0xB1	Revision B1

Byte 140 (0x08C) (Load Reduced): DRAM VrefDQ for Package Rank 0

This byte defines the VrefDQ value for the package rank 0 DRAMs.

Reserved		DRAM VrefDQ for package rank 0 DRAMs					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Encoding matches MR6 A5:A0 encoding in the JESD79-4 specification.					
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Byte 141 (0x08D) (Load Reduced): DRAM VrefDQ for Package Rank 1

This byte defines the VrefDQ value for the package rank 1 DRAMs.

Reserved		DRAM VrefDQ for package rank 1 DRAMs					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Encoding matches MR6 A5:A0 encoding in the JESD79-4 specification.					
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Byte 142 (0x08E) (Load Reduced): DRAM VrefDQ for Package Rank 2

This byte defines the VrefDQ value for the package rank 2 DRAMs.

Reserved		DRAM VrefDQ for package rank 2 DRAMs					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Encoding matches MR6 A5:A0 encoding in the JESD79-4 specification.					
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Byte 143 (0x08F) (Load Reduced): DRAM VrefDQ for Package Rank 3

This byte defines the VrefDQ value for the package rank 3 DRAMs.

Reserved		DRAM VrefDQ for package rank 3 DRAMs					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Encoding matches MR6 A5:A0 encoding in the JESD79-4 specification.					
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Byte 144 (0x090) (Load Reduced): Data Buffer VrefDQ for DRAM Interface

This byte defines the DRAM interface VrefDQ value for the data buffer component.

Data Buffer VrefDQ for DRAM Interface							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
For encoding see definition of F5BC6x (DRAM Interface VREF Control word) in the DDR4DB01 specification.							
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Byte 145 (0x091) (Load Reduced): Data Buffer MDQ Drive Strength and RTT for data rate ≤ 1866

This byte defines the drive strength for MDQ/MDQS outputs and the Read RTT termination strength of the data buffer component.

Data Buffer MDQ Drive Strength and RTT							
DRAM Interface MDQ Drive Strength				DRAM Interface MDQ Read Termination Strength			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	000 = RZQ/6 (40 Ω) 001 = RZQ/7 (34 Ω) 010 = RZQ/5 (40 Ω) 011 = Reserved 100 = Reserved 101 = RZQ/4 (60 Ω) 110 = Reserved 111 = Reserved			Reserved	000 = Disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ (240 Ω) 101 = RZQ/5 (40 Ω) 110 = RZQ/3 (80 Ω) 111 = RZQ/7 (34 Ω)		
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Byte 146 (0x092) (Load Reduced): Data Buffer MDQ Drive Strength and RTT for 1866 < data rate ≤ 2400

This byte defines the drive strength for MDQ/MDQS outputs and the Read RTT termination strength of the data buffer component.

Data Buffer MDQ Drive Strength and RTT							
DRAM Interface MDQ Drive Strength				DRAM Interface MDQ Read Termination Strength			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	000 = RZQ/6 (40 Ω) 001 = RZQ/7 (34 Ω) 010 = RZQ/5 (40 Ω) 011 = Reserved 100 = Reserved 101 = RZQ/4 (60 Ω) 110 = Reserved 111 = Reserved			Reserved	000 = Disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ (240 Ω) 101 = RZQ/5 (40 Ω) 110 = RZQ/3 (80 Ω) 111 = RZQ/7 (34 Ω)		
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Byte 147 (0x093) (Load Reduced): Data Buffer MDQ Drive Strength and RTT for 2400 < data rate ≤ 3200

This byte defines the drive strength for MDQ/MDQS outputs and the Read RTT termination strength of the data buffer component.

Data Buffer MDQ Drive Strength and RTT							
DRAM Interface MDQ Drive Strength				DRAM Interface MDQ Read Termination Strength			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	000 = RZQ/6 (40 Ω) 001 = RZQ/7 (34 Ω) 010 = RZQ/5 (40 Ω) 011 = Reserved 100 = Reserved 101 = RZQ/4 (60 Ω) 110 = Reserved 111 = Reserved			Reserved	000 = Disabled 001 = RZQ/6 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/4 (40 Ω) 100 = RZQ (240 Ω) 101 = RZQ/5 (40 Ω) 110 = RZQ/3 (80 Ω) 111 = RZQ/7 (34 Ω)		
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Byte 148 (0x094) (Load Reduced): DRAM Drive Strength (for data rates ≤ 1866, 1866 < data rate ≤ 2400, and 2400 < data rate ≤ 3200)

This byte defines the output buffer drive strength for the DRAMs.

DRAM Drive Strength							
Reserved		2400 < Data rate ≤ 3200		1866 < Data rate ≤ 2400		Data rate ≤ 1866	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		00 = RZQ/7 (34 Ω) 01 = RZQ/5 (40 Ω) 10 = Reserved 11 = Reserved		00 = RZQ/7 (34 Ω) 01 = RZQ/5 (40 Ω) 10 = Reserved 11 = Reserved		00 = RZQ/7 (34 Ω) 01 = RZQ/5 (40 Ω) 10 = Reserved 11 = Reserved	
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Byte 149 (0x095) (Load Reduced): DRAM ODT (RTT_WR and RTT_NOM) for data rate ≤ 1866

This byte defines the ODT termination strength for the DRAMs.

DRAM ODT Strength							
Reserved		RTT_WR			RTT_NOM		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		000 = Dynamic ODT Off 001 = RZQ/2 (120 Ω) 010 = RZQ (240 Ω) 011 = Hi-Impedance 100 = RZQ/3 (80 Ω) 101 = Reserved 110 = Reserved 111 = Reserved			000 = Disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ (240 Ω) 101 = RZQ/5 (40 Ω) 110 = RZQ/3 (80 Ω) 111 = RZQ/7 (34 Ω)		
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Byte 150 (0x096) (Load Reduced): DRAM ODT (RTT_WR and RTT_NOM) for 1866 < data rate ≤ 2400

This byte defines the ODT termination strength for the DRAMs.

DRAM ODT Strength							
Reserved		RTT_WR			RTT_NOM		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		000 = Dynamic ODT Off 001 = RZQ/2 (120Ω) 010 = RZQ (240 Ω) 011 = Hi-Impedance 100 = RZQ/3 (80 Ω) 101 = Reserved 110 = Reserved 111 = Reserved			000 = Disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ (240 Ω) 101 = RZQ/5 (40 Ω) 110 = RZQ/3 (80 Ω) 111 = RZQ/7 (34 Ω)		
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Byte 151 (0x097) (Load Reduced): DRAM ODT (RTT_WR and RTT_NOM) for 2400 < data rate ≤ 3200

This byte defines the ODT termination strength for the DRAMs.

DRAM ODT Strength							
Reserved		RTT_WR			RTT_NOM		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		000 = Dynamic ODT Off 001 = RZQ/2 (120Ω) 010 = RZQ (240 Ω) 011 = Hi-Impedance 100 = RZQ/3 (80 Ω) 101 = Reserved 110 = Reserved 111 = Reserved			000 = Disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ (240 Ω) 101 = RZQ/5 (40 Ω) 110 = RZQ/3 (80 Ω) 111 = RZQ/7 (34 Ω)		
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Byte 152 (0x098) (Load Reduced): DRAM ODT (RTT_PARK) for data rate ≤ 1866

This byte defines the ODT termination strength for the DRAMs.

DRAM ODT Strength							
Reserved		RTT_PARK, Package Ranks 2 & 3			RTT_PARK, Package Ranks 0 & 1		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		000 = Disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ (240 Ω) 101 = RZQ/5 (40 Ω) 110 = RZQ/3 (80 Ω) 111 = RZQ/7 (34 Ω)			000 = Disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ (240 Ω) 101 = RZQ/5 (40 Ω) 110 = RZQ/3 (80 Ω) 111 = RZQ/7 (34 Ω)		
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Byte 153 (0x099) (Load Reduced): DRAM ODT (RTT_PARK) for 1866 < data rate ≤ 2400

This byte defines the ODT termination strength for the DRAMs.

DRAM ODT Strength							
Reserved		RTT_PARK, Package Ranks 2 & 3			RTT_PARK, Package Ranks 0 & 1		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		000 = Disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ (240 Ω) 101 = RZQ/5 (40 Ω) 110 = RZQ/3 (80 Ω) 111 = RZQ/7 (34 Ω)			000 = Disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ (240 Ω) 101 = RZQ/5 (40 Ω) 110 = RZQ/3 (80 Ω) 111 = RZQ/7 (34 Ω)		
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Byte 154 (0x09A) (Load Reduced): DRAM ODT (RTT_PARK) for 2400 < data rate ≤ 3200

This byte defines the ODT termination strength for the DRAMs.

DRAM ODT Strength							
Reserved		RTT_PARK, Package Ranks 2 & 3			RTT_PARK, Package Ranks 0 & 1		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		000 = Disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ (240 Ω) 101 = RZQ/5 (40 Ω) 110 = RZQ/3 (80 Ω) 111 = RZQ/7 (34 Ω)			000 = Disabled 001 = RZQ/4 (60 Ω) 010 = RZQ/2 (120 Ω) 011 = RZQ/6 (40 Ω) 100 = RZQ (240 Ω) 101 = RZQ/5 (40 Ω) 110 = RZQ/3 (80 Ω) 111 = RZQ/7 (34 Ω)		
Note 1 Standard values are defined in the DDR4 LRDIMM Reference Design Annexes for JEDEC standard module reference designs.							

Bytes 155~253 (0x09B~0x0FD) (Load Reduced):

Reserved -- must be coded as 0x00

Bytes 254 (0x0FE) (Load Reduced): Cyclical Redundancy Code (CRC) for Module Specific Section, LSB

Bytes 255 (0x0FF) (Load Reduced): Cyclical Redundancy Code (CRC) for Module Specific Section, MSB

This two-byte field contains the calculated CRC for bytes 128~253 (0x080~0x0FD) in the SPD. See bytes 126~127 for coding example.