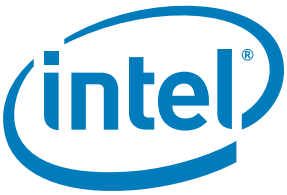

Intel® Extreme Memory Profile (XMP)

Specification

Enthusiast Extension to the JEDEC DDR3 SPD Specification

Rev 1.1

October 2007

Revision History

Date	Rev	Pages	Contents of Modification
March 23, 2007	0.1	All	First Draft.
April 16, 2007	0.5	All	Corrected multiple pages for misc errors, reformatted a few bytes to allow forward flexibility. Some bytes now not MTB devised. More examples put in (Future drafts will complete the mobile oriented bytes and give more examples of speedbins outside of the standard)
May 2, 2007	0.6	All	Corrected duplicated byte 186 -tCKmin. Corrected text for byte 190 - tCWL. Added push-out capability to the turn around time bytes, also corrected the back to back turn around time byte to the proper byte number, was referenced as the same as the previous byte. Added clarification to several bytes on the DDR3 design limitations - such as tWTR, which is limited by design to 4tCK min.
May 30, 2007	0.7	All	Corrected the misc Hex conversion errors and misc typo's in the document
June 28, 2007	1.0	All	Updated specification name.
July 9, 2007	1.01	20,25,26, 27	tRFC incorrectly noted in nS, changed to uS. Turn around byte 206, 241, 207, 242 missing default setting, re-configured to assign appropriately. Added default mode to CMD rate Byte(s) 208/243
Aug 15, 2007	1.02	Multiple	Added verbiage to discuss how Profile 1 and Profile 2 are used. Profile 1 is the Enthusiast / Certified profile and is what is tested under the XMP certification program. Profile 2 is designed to host the Extreme / 'no holds barred' settings that most likely will not have the stability of the first profile. This profile is for the purist or extreme over-clocker that may just want to know what the absolute best parameters are that the DIMM supports.
Sept 21, 2007	1.03	Multiple	Declassified Spec. Corrected multiple spelling errors. Added additional information to discuss the purpose of XMP.
Oct 1, 2007	1.04	Page 9	Defined Byte 178 - Profile Organization.
Oct 31, 2007	1.1	Multiple	ALLCHANGES ARE IN RED. Re-defined Byte 178 - Profile Organization to add support for # of DIMMs per CH, also added seperate MTB divisor/dividend for Profile 2 - this will allow different frequencies to be easily supported on the 2nd profile. Also added a resvered byte for vendor use to the end of each profile - Byte 219/ Byte 254. These bytes are for special use between Module vendors and OEMs/ODMs. Consider these bytes Vendor Personality Bytes.

Appendix X: *Intel Extreme Memory Profile* Serial Presence Detect (SPD) for DDR3 SDRAM Modules

1.0 Introduction

Intel Extreme Memory provides a simple and robust high performance, DDR3 based memory solution for Intel based platforms. Modules are designed around this specification. The XMP Spec was developed by Intel and it's memory partners to enable a enthusiast performance extension to the traditional JEDEC SPD Spec.

Intel Extreme Memory Profiles are traditionally designed with two performance profiles. Profile 1 is used for the Enthusiast / Certified settings and is the profile that is tested under the Intel Extreme Memory Certification program. Profile 2 is designed to host the Extreme or Fastest possible settings that have no guardband and may or may not work on every system.

It should also be noted that Extreme Memory Profiles aren't always defined as over-frequency / over-voltaged parts. In some cases, Extreme Memory Profiles can be used to define Extremely power savvy settings or Extremely fast latencies.

Intel Extreme Memory end user benefits

- Enables users to take advantage of the fastest DDR3 memory
- Provides a mechanism for end users to easily performance tune Intel platforms
- Enables both novice (use built-in profiles) and advanced users (manually adjust timing parameters) to performance tune their Intel platforms.

Intel Extreme Memory DIMM vendor benefits

- Ability for DIMM vendors to provide value added capability and performance optimizations
- Enable DIMM vendors to differentiate Extreme Memory, designed specifically for enthusiasts, gamers and over-clockers from other memory.

This appendix describes the *Intel Extreme Memory Profile* serial presence detect (SPD) values for all DDR3 modules. These presence detect values are those referenced in the SPD standard document for 'Specific Features' and are in some cases, are features outside of the standard. The following SPD fields will be documented in the order presented in section 1.1. All unused entries will be coded as 00h. All unused bits in defined bytes will be coded as 0 except where noted.

To allow for maximum flexibility as devices evolve, SPD fields described in this document may support device configuration and timing options that are not included in the JEDEC DDR3 SDRAM data sheet (JESD79-3). Please refer to DRAM supplier data sheets or JESD79-3 to determine the compatibility of components.

1.1 Address map

The following is the SPD address map for all DDR3 modules. It describes where the individual lookup table entries will be held in the serial EEPROM.

Byte Number	Function Described	Notes
176-177	*Intel Extreme Memory Profile* ID String	
178	*Intel Extreme Memory Profile* Organization Type	
179	*Intel Extreme Memory Profile* Revision	
180	Medium Timebase Dividend for Profile 1	1
181	Medium Timebase Divisor for Profile 1	1
182	Medium Timebase Dividend for Profile 2	1
183	Medium Timebase Divisor for Profile 2	1
184	RSVD	1
185	Module VDD Voltage Level for Profile 1 (Certified Settings)	1
186	SDRAM Minimum Cycle Time (tCKmin)	2,4
187	Minimum CAS Latency Time (tAAmin)	2,4
188	CAS Latencies Supported, Least Significant Byte (CL MASK)	2,4
189	CAS Latencies Supported, Most Significant Byte (CL MASK)	2,4
190	Minimum CAS Write Latency Time (tCWLmin)	2
191	Minimum Row Precharge Time (tRPmin)	2,4
192	Minimum RAS# to CAS# Delay Time (tRCDmin)	2,4
193	Minimum Write Recovery Time (tWRmin)	2,4
194	Upper Nibbles for tRAS and tRC	2,4
195	Minimum Active to Precharge Time (tRASmin), Least Significant Byte	2,4
196	Minimum Active to Active/Refresh Time (tRCmin), Least Significant Byte	2,4
197	Maximum tREFI Time (Average Periodic Refresh Interval) - LSB	2
198	Maximum tREFI Time (Average Periodic Refresh Interval) - MSB	2
199	Minimum Refresh Recovery Time (tRFCmin), Least Significant Byte	2,4
200	Minimum Refresh Recovery Time (tRFCmin), Most Significant Byte	2,4
201	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	2,4
202	Minimum Row Active to Row Active Delay Time (tRRDmin)	2,4

1. Global Parameters used across all profiles
2. Utilized for Profile 1 (Enthusiast / Certified Settings)
3. Utilized for Profile 2 (Extreme Settings)
4. Parameter utilized in the same fashion as the standard DDR3 SPD byte with the exception that it may exceed the DDRx SDRAM datasheet

Byte Number	Function Described	Notes
203	Upper Nibble for tFAW	2,4
204	Minimum Four Activate Window Delay Time (tFAWmin)	2,4
205	Minimum Internal Write to Read Command Delay Time (tWTRmin)	2,4
206	Write to Read & Read to Write CMD Turn-around Time Pull-in	2
207	Back to Back CMD Turn-around Time Pull-in	2
208	System ADD/CMD Rate (1N or 2N mode)	2
209	Auto Self Refresh Performance (Sub 1x Refresh and IDD6 Impacts)	2
210-218	RSVD	2
219	Vendor Personality Byte for Profile 1 - RSVD	3,4
220	Module VDD Voltage Level for Profile 2 (Extreme Settings)	3,4
221	SDRAM Minimum Cycle Time (tCKmin)	3,4
222	Minimum CAS Latency Time (tAAmin)	3,4
223	CAS Latencies Supported, Least Significant Byte (CL MASK)	3,4
224	CAS Latencies Supported, Most Significant Byte (CL MASK)	3
225	Minimum CAS Write Latency Time (tCWLmin)	3,4
226	Minimum Row Precharge Time (tRPmin)	3,4
227	Minimum RAS# to CAS# Delay Time (tRCDmin)	3,4
228	Minimum Write Recovery Time (tWRmin)	3,4
229	Upper Nibbles for tRAS and tRC	3,4
230	Minimum Active to Precharge Time (tRASmin), Least Significant Byte	3,4
231	Minimum Active to Active/Refresh Time (tRCmin), Least Significant Byte	3
232	Maximum tREFI Time (Average Periodic Refresh Interval) - LSB	3
233	Maximum tREFI Time (Average Periodic Refresh Interval) - MSB	3,4
234	Minimum Refresh Recovery Time (tRFCmin), Least Significant Byte	3,4
235	Minimum Refresh Recovery Time (tRFCmin), Most Significant Byte	3,4
236	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	3,4
237	Minimum Row Active to Row Active Delay Time (tRRDmin)	3,4
238	Upper Nibble for tFAW	3,4
239	Minimum Four Activate Window Delay Time (tFAWmin)	3,4

1. Global Parameters used across all profiles
2. Utilized for Profile 1 (Enthusiast / Certified Settings)
3. Utilized for Profile 2 (Extreme Settings)
4. Parameter utilized in the same fashion as the standard DDR3 SPD byte with the exception that it may exceed the DDRx SDRAM datasheet

Byte Number	Function Described	Notes
240	Minimum Internal Write to Read Command Delay Time (tWTRmin)	3
241	Write to Read & Read to Write CMD Turn-around Time Pull-in	3
242	Back to Back CMD Turn-around Time Pull-in	3
243	System ADD/CMD Rate (1N or 2N mode)	3
244	Auto Self Refresh Performance (Sub 1x Refresh and IDD6 Impacts)	3
245-253	RSVD	3
254	Vendor Personality Byte for Profile 2 - RSVD	3

1. Global Parameters used across all profiles
2. Utilized for Profile 1 (Enthusiast / Certified Settings)
3. Utilized for Profile 2 (Extreme Settings)
4. Parameter utilized in the same fashion as the standard DDR3 SPD byte with the exception that it may exceed the DDRx SDRAM datasheet

2.0 Details of each byte

Important Note: Throughout this document, you will find that in order to save space, the descriptions of the bytes were not replicated when they were the same. This will be done by listing both or all byte numbers near the title of each byte. For example: Byte 186 or 221: Minimum SDRAM Cycle Time (t_{CK}min). This title indicates that both Byte 186 and Byte 221 are used for tCKmin values and should be programmed the same way. Byte 186 is for the first profile, while Byte 221 is for the 2nd profile.

All bytes not programmed or RSVD MUST be programmed at 0 (zero). This is a standard SPD programming protocol.

2.1 Global Section: Bytes 176 to 184

This section contains defines bytes that are common to all extended mode profiles.

Byte 176 or 177: *Intel Extreme Memory Profile* Identification String

Two bytes are required to ensure that the module supports the correct performance mode and isn't populated with some other customer data. Potentially this string could be used to identify incompatibility between different designs.

Line #	SDRAM / Module Type Corresponding to Key Byte	Byte 176 [7:0]								Byte 177 [7:0]								
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Intel Extreme Memory Profile ID String	0	0	0	0	1	1	0	0	0	1	0	0	1	0	1	0	0C4A
-		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
253	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	FFFD
254	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	FFFE
255	Reserved	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF

Byte 178: *Intel Extreme Memory Profile* Organization & Configuration

This byte is primary utilized to inform the platform about which profiles are programmed and what configuration they are designed for. In some cases, suppliers may choose not to populate profile 2 and to avoid system BIOS confusion, bits 0 & 1 were defined. Bits 2 through 5 define the recommended channel configuration for each profile. The rest of the bits of this byte may be used in the future to define different profile organizations for a specific profile ID.

Bit 7 ~ Bit 6	Bits 5-4	Bits 3-2	Bit 1	Bit 0
Reserved	Profile 2 Recommended Channel Config	Profile 1 Recommended Channel Config	Profile 2 Enabled	Profile 1 Enabled
Reserved[1]	00 - 1 DIMM per CH 01 - 2 DIMM per CH 10 - 3 DIMM per CH 11 - 4 DIMM per CH	00 - 1 DIMM per CH 01 - 2 DIMM per CH 10 - 3 DIMM per CH 11 - 4 DIMM per CH	0 - Disabled 1 - Enabled	0 - Disabled 1 - Enabled[2]

NOTES:
1. Reserved bytes must be programmed to 0 (zero)
2. Bit 0 must always be programmed to 1 - Profile 1 must always be enabled

Byte 179: *Intel Extreme Memory Profile* Revision

This byte describes the compatibility level of the *Intel Extreme Memory Profile* encoding of the bytes contained in the SPD EEPROM, and the current collection of valid defined bytes. This byte will be coded as 0x10 for SPDs with *Intel Extreme Memory Profile* revision level 1.0. Software should examine the upper nibble (Encoding Level or Major Revision Level) to determine if it can correctly interpret the contents of the module SPD. The lower nibble (Additions Level or Minor Revision Level) can optionally be used to determine which additional bytes or attribute bits have been defined since introduction of the major revision level. Historically, Encoding Levels or Major Revision levels are rare and only introduced when some feature is added that potentially breaks backward compatibility or significant changes have taken place since introduction of that major revision number, in all other cases, an additions level or minor revision level is just added to the revision number. **This should now be programmed as Rev1.1**

Intel Extreme Memory Profile Revision	Encoding Level				Additions Level				Hex
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Revision 0.0	0	0	0	0	0	0	0	0	00
Revision 0.1	0	0	0	0	0	0	0	1	01
...	.	.	.	.	.	.	.	.	.
Revision 1.0	0	0	0	1	0	0	0	0	10
Revision 1.1	0	0	0	1	0	0	0	1	11
...	.	.	.	.	.	.	.	.	...
Undefined	1	1	1	1	1	1	1	1	FF

Byte 180: Medium Timebase (MTB) Dividend for Profile 1
Byte 181: Medium Timebase (MTB) Divisor for Profile 1

These bytes define a value in nanoseconds that represents the fundamental timebase for medium grain timing calculations. This value is typically the greatest common divisor for the range of clock frequencies (clock periods) supported by a particular SDRAM. This value is used as a multiplier for formulating subsequent timing parameters. The medium timebase (MTB) is defined as the medium timebase dividend (byte 180) divided by the medium timebase divisor (byte 181).

For legacy applications (platforms that use XMP Rev1.0), Bytes 180/181 will define the MTB for both profiles 1 and 2. The system should utilize Byte 179 (Rev#) to avoid conflicts.

Byte 180 Bit 7 ~ Bit 0	Byte 181 Bit 7 ~ Bit 0
Medium Timebase (MTB) Dividend	Medium Timebase (MTB) Divisor
Values defined from 1 to 255	Values defined from 1 to 255

Examples:

Dividend	Divisor	Timebase (ns)	Use
1	8	0.125	For clock frequencies of 400, 533, 667, and 800 MHz

To simplify BIOS implementation, DIMMs associated with a given key byte value may differ in MTB value only by a factor of two. For DDR3 modules, the defined MTB values are

:

Dividend	Divisor	Timebase (ns)	Use
1	8	0.125	MTB Value for DDR3
1	12	0.083333	Example of use for finer control
1	16	0.0625	Example of use for finer control

Details of how these could be used can be seen in the examples of Byte 186 (tCKmin)

Byte 182: Medium Timebase (MTB) Dividend for Profile 2
Byte 183: Medium Timebase (MTB) Divisor for Profile 2

These bytes define a value in nanoseconds that represents the fundamental timebase for medium grain timing calculations. This value is typically the greatest common divisor for the range of clock frequencies (clock periods) supported by a particular SDRAM. This value is used as a multiplier for formulating subsequent timing parameters. The medium timebase (MTB) is defined as the medium timebase dividend (byte 182) divided by the medium timebase divisor (byte 183).

Byte 182 Bit 7 ~ Bit 0	Byte 183 Bit 7 ~ Bit 0
Medium Timebase (MTB) Dividend	Medium Timebase (MTB) Divisor
Values defined from 1 to 255	Values defined from 1 to 255

Examples:

Dividend	Divisor	Timebase (ns)	Use
1	8	0.125	For clock frequencies of 400, 533, 667, and 800 MHz

To simplify BIOS implementation, DIMMs associated with a given key byte value may differ in MTB value only by a factor of two. For DDR3 modules, the defined MTB values are

:

Dividend	Divisor	Timebase (ns)	Use
1	8	0.125	MTB Value for DDR3
1	12	0.083333	Example of use for finer control
1	16	0.0625	Example of use for finer control

Details of how these could be used can be seen in the examples of Byte 186 (tCKmin)

Byte 184: Reserved Global Byte

Byte 185 or 220: Module VDD Voltage Level

This byte describes the Modules VDD Voltage Level for Profiles 1 and 2. The Byte will allow voltages above and below the typical standard voltage for Overclocking and Low Power Performance Modes. This byte does not use MTB.

Voltage	Bits(6:5) show the integer of the voltage							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0.0V	RSVD	0	0	See Subfield B				
1.0V		0	1					
2.0V		1	0					
Undefined		1	1					

Voltage	Bits(4:0) show the decimal fraction of the voltage							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0.00V	RSVD	See Subfield A		0	0	0	0	0
0.05V				0	0	0	0	1
0.10V				0	0	0	1	0
0.15V				0	0	0	1	1
0.20V				0	0	1	0	0
0.25V				0	0	1	0	1
0.30V				0	0	1	1	0
0.35V				0	0	1	1	1
0.40V				0	1	0	0	0
0.45V				0	1	0	0	1
0.50V				0	1	0	1	0
0.55V				0	1	0	1	1
0.60V				0	1	1	0	0
0.65V				0	1	1	0	1
0.70V				0	1	1	1	0
0.75V				0	1	1	1	1
0.80V				1	0	0	0	0
0.85V				1	0	0	0	1
0.90V				1	0	0	1	0
0.95V				1	0	0	1	1
Undefined				All other combinations				

Examples:

RSVD Field	Subfield A Binary Value	Subfield B Binary Value	Hex Value programmed	Use
0	01	00111	27h	Low Power DDR3 @ 1.35V VDD
0	10	00001	41h	Overvoltage DDR3 @ 2.05V VDD

Note: Non-used / RSVD bytes are always programmed by default at zero.

Byte 186 or 221: Minimum SDRAM Cycle Time (t_{CK}min)

This byte defines the minimum cycle time for the SDRAM module, in medium timebase (MTB) units. This number applies to all applicable components on the module. This byte applies to SDRAM and support components as well as the overall capability of the DIMM. This value is based off but may exceed the DDR3 SDRAM data sheet.

Bit 7 ~ Bit 0
Minimum SDRAM Cycle Time (t_{CK}min) MTB Units
Values defined from 1 to 255

Examples with Dividend of 1 and Divisor of 8:

tCKmin (MTB units)	Timebase (ns)	tCKmin Result (ns)	Use
20	0.125	2.5	DDR3 with 400 MHz clock - 800MT/s
15	0.125	1.875	DDR3 with 533 MHz clock - 1066MT/s
12	0.125	1.5	DDR3 with 667 MHz clock - 1333MT/s
10	0.125	1.25	DDR3 with 800 MHz clock - 1600MT/s

Examples with Dividend of 1 and Divisor of 12:

tCKmin (MTB units)	Timebase (ns)	tCKmin Result (ns)	Use
19	0.083333	1.5833	DDR3 with 631 MHz clock - 1263MT/s
18	0.083333	1.5	DDR3 with 667 MHz clock - 1333MT/s
16	0.083333	1.3333	DDR3 with 750 MHz clock - 1500MT/s
15	0.083333	1.25	DDR3 with 800 MHz clock - 1600MT/s
14	0.083333	0.8571	DDR3 with 857 MHz clock - 1714MT/s

Examples with Dividend of 1 and Divisor of 16:

tCKmin (MTB units)	Timebase (ns)	tCKmin Result (ns)	Use
25	0.0625	1.5625	DDR3 with 640 MHz clock - 1280MT/s
24	0.0625	1.5	DDR3 with 667 MHz clock - 1333MT/s
21	0.0625	1.3125	DDR3 with 761 MHz clock - 1523MT/s
20	0.0625	1.25	DDR3 with 800 MHz clock - 1600MT/s
15	0.0625	0.9375	DDR3 with 1066 MHz clock - 2133MT/s

Byte 187 or 222: Minimum CAS Latency Time (t_{AA}min)

This byte defines the minimum CAS Latency in medium timebase (MTB) units. Software can use this information, along with the CAS Latencies supported (found in bytes 188/223 and 189/224) to determine the optimal cycle time for a particular module. This value is based off but may exceed the DDR3 SDRAM data sheet.

Bit 7 ~ Bit 0
Minimum SDRAM CAS Latency Time (t_{AA}min) MTB Units
Values defined from 1 to 255

Examples:

tAAmin (MTB units)	Timebase (ns)	tAAmin Result (ns)	Use
100	0.125	12.5	DDR3-800D
120	0.125	15	DDR3-800E
90	0.125	11.25	DDR3-1066E
105	0.125	13.125	DDR3-1066F
120	0.125	15	DDR3-1066G
84	0.125	10.5	DDR3-1333F
96	0.125	12	DDR3-1333G
108	0.125	13.5	DDR3-1333H
120	0.125	15	DDR3-1333J
80	0.125	10	DDR3-1600G
90	0.125	11.25	DDR3-1600H
100	0.125	12.5	DDR3-1600J
110	0.125	13.75	DDR3-1600K

CAS Latency Calculation and Examples

CAS latency is not a purely analog value as DDR3 SDRAMs use the DLL to synchronize data and strobe outputs with the clock. All possible frequencies may not be tested, therefore an application should use the next smaller JEDEC standard tCKmin value (2.5, 1.875, 1.5, or 1.25 ns for DDR3 SDRAMs) when calculating CAS Latency. This section shows how the BIOS may calculate CAS latency based on Bytes 12 ~ 16.

Step 1: Determine the common set of supported CAS Latency values for all modules on the memory channel using the CAS Latencies Supported in SPD bytes 14 and 15.

Step 2: Determine tAAmin(all) which is the largest tAAmin value for all modules on the memory channel (SPD byte 16).

Step 3: Determine tCKmin(all) which is the largest tCKmin value for all modules on the memory channel (SPD byte 12).

Step 4: For a proposed tCK value (tCKproposed) between tCKmin(all) and tCKmax, determine the desired CAS Latency. If tCKproposed is not a standard JEDEC value (2.5, 1.875, 1.5, or 1.25 ns) then tCKproposed must be adjusted to the next lower standard tCK value for calculating CLdesired.

CLdesired = ceiling (tAAmin(all) / tCKproposed)

where tAAmin is defined in Byte 16. The ceiling function requires that the quotient be rounded up always.

Step 5: Chose an actual CAS Latency (CLactual) that is greater than or equal to CLdesired and is supported by all modules on the memory channel as determined in step 1. If no such value exists, choose a higher tCKproposed value and repeat steps 4 and 5 until a solution is found.

Step 6: Once the calculation of CLactual is completed, the BIOS must also verify that this CAS Latency value does not exceed tAAmax, which is 20 ns for all DDR3 speed grades, by multiplying CLactual times tCKproposed. If not, choose a lower CL value and repeat steps 5 and 6 until a solution is found.

Example 1: Slot 0 = DDR3-1066E 6-6-6, Slot 1 = DDR3-1333H 9-9-9

Step 1: CL in slot 0 = 5, 6, 7, 8; CL in slot 1 = 6, 8, 9; Common CL = 6, 8
Step 2: tAAmin in slot 0 = 11.25 ns; tAAmin in slot 1 = 13.5 ns; tAAmin(all) = 13.5 ns
Step 3: tCKmin in slot 0 = 1.875 ns; tCKmin in slot 1 = 1.5 ns; tCKproposed = 1.875 ns
Step 4: CLdesired = ceiling(13.5 / 1.875) = 8
Step 5: CLactual = CLdesired
Step 6: CLactual * tCKproposed = 8 * 1.875 = 15 < 20 ns ... value is okay
Results: tCKactual = 1.875 ns, CLactual = 8

Example 2: Slot 0 = DDR3-800D 5-5-5, Slot 1 = DDR3-1066G 8-8-8

Step 1: CL in slot 0 = 5, 6; CL in slot 1 = 6, 8; Common CL = 6
Step 2: tAAmin in slot 0 = 12.5 ns; tAAmin in slot 1 = 15 ns; tAAmin(all) = 15 ns
Step 3: tCKmin in slot 0 = 2.5 ns; tAAmin in slot 1 = 1.875 ns; tCKproposed = 2.5 ns
Step 4: CLdesired = ceiling(15 / 2.5 ns) = 6
Step 5: CLactual = CLdesired
Step 6: CLactual * tCKproposed = 6 * 2.5 = 15 < 20 ns ... value is okay
Results: tCKactual = 2.5 ns, CLactual = 6

Example 3: Slot 0 = DDR3-800D 5-5-5, Slot 1 = DDR3-1066G 8-8-8, System Bringup & Debug limits operating frequency to 333 MHz (tCK = 3.3 ns)

Step 1: CL in slot 0 = 5, 6; CL in slot 1 = 6, 8; Common CL = 6
Step 2: tAAmin in slot 0 = 12.5 ns; tAAmin in slot 1 = 15 ns; tAAmin(all) = 15 ns
Step 3: tCKproposed = 3.3 ns
Step 4: CLdesired = ceiling(15 / 3.3 ns) = 5
Step 5: CLactual = 6
Step 6: CLactual * tCKproposed = 6 * 3.3 = 19.8 < 20 ns ... value is okay
Results: tCKactual = 3.3 ns, CLactual = 6

Byte 188 or 223: CAS Latencies Supported, Low Byte

Byte 189 or 224: CAS Latencies Supported, High Byte

These bytes define which CAS Latency (CL) values are supported. The range is from CL = 4 through CL = 18 with one bit per possible CAS Latency. A 1 in a bit position means that CL is supported, a 0 in that bit position means it is not supported. Since CL = 6 is required for all DDR3 speed bins, bit 2 of SPD byte 188 or 223 is always 1. Typical use for this set of bytes in the enthusiast market would be to enable every byte for flexibility though you may find it necessary to limit certain configs for stability. This value is based off but may exceed the DDR3 SDRAM data sheet.

Byte 188/223: CAS Latencies Supported, Low Byte							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CL = 11	**CL = 10**	**CL = 9**	**CL = 8**	**CL = 7**	**CL = 6**	**CL = 5**	**CL = 4**
0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	1	0 or 1	0 or 1
Byte 189/224: CAS Latencies Supported, High Byte							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Reserved	**CL = 18**	**CL = 17**	**CL = 16**	**CL = 15**	**CL = 14**	**CL = 13**	**CL = 12**
0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
For each bit position, 0 means this CAS Latency is not supported, 1 means this CAS Latency is supported.							

Example: DDR3-1600K

Byte 188 or 223 = 0xD4 (= 1101 0100) -- low byte.

Byte 189 or 224 = 0x00 (= 0000 0000) -- high byte.

CAS Latencies	**x**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**
CL Mask	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**1**	**0**	**0**

Results: Actual CAS Latencies supported = 6, 8, 10, and 11.

Byte 190 or 225: Minimum CAS Write Latency Time (t_{CWL}min)

This byte defines the minimum CAS Write Latency in medium timebase (MTB) units. This value is based off but may exceed the DDR3 SDRAM data sheet. Programmed in the same fashion as tRPmin.

Bit 7 ~ Bit 0
Minimum SDRAM CAS Write Latency Time (t_{CWL}min) MTB Units
Values defined from 1 to 255

Byte 191 or 226: Minimum Row Precharge Delay Time (t_{RP}min)

This byte defines the minimum SDRAM Row Precharge Delay Time in medium timebase (MTB) units. This value is based off but may exceed the DDR3 SDRAM data sheet.

Bit 7 ~ Bit 0
Minimum Row Precharge Time (t_{RP}) MTB Units
Values defined from 1 to 255

Examples:

Hex	tRP (MTB units)	Timebase (ns)	tRP Result (ns)	Use
65	100	0.125	12.5	DDR3-800D
78	120	0.125	15	DDR3-800E
5A	90	0.125	11.25	DDR3-1066E
69	105	0.125	13.125	DDR3-1066F
78	120	0.125	15	DDR3-1066G
54	84	0.125	10.5	DDR3-1333F
60	96	0.125	12	DDR3-1333G
6C	108	0.125	13.5	DDR3-1333H
78	120	0.125	15	DDR3-1333J
50	80	0.125	10	DDR3-1600G
5A	90	0.125	11.25	DDR3-1600H
65	100	0.125	12.5	DDR3-1600J
6E	110	0.125	13.75	DDR3-1600K

Byte 192 or 227: Minimum RAS# to CAS# Delay Time (t_{RCD}min)

This byte defines the minimum SDRAM RAS# to CAS# Delay in medium timebase (MTB) units. This value is based off but may exceed the DDR3 SDRAM data sheet.

Bit 7 ~ Bit 0
Minimum RAS# to CAS# Delay (t_{RCD}) MTB Units
Values defined from 1 to 255

Examples:

Hex	tRCD (MTB units)	Timebase (ns)	tRCD Result (ns)	Use
65	100	0.125	12.5	DDR3-800D
78	120	0.125	15	DDR3-800E
5A	90	0.125	11.25	DDR3-1066E
69	105	0.125	13.125	DDR3-1066F
78	120	0.125	15	DDR3-1066G
54	84	0.125	10.5	DDR3-1333F
60	96	0.125	12	DDR3-1333G
6C	108	0.125	13.5	DDR3-1333H
78	120	0.125	15	DDR3-1333J
50	80	0.125	10	DDR3-1600G
5A	90	0.125	11.25	DDR3-1600H
65	100	0.125	12.5	DDR3-1600J
6E	110	0.125	13.75	DDR3-1600K

Byte 193 or 228: Minimum Write Recovery Time (t_{WR}min)

This byte defines the minimum SDRAM write recovery time in medium timebase (MTB) units. This value is based off but may exceed the DDR3 SDRAM data sheet.

Bit 7 ~ Bit 0
Minimum Write Recovery Time (t_{WR}) MTB Units
Values defined from 1 to 255

Example:

tWRmin (MTB units)	Timebase (ns)	tWR Result (ns)	Use
120	0.125	15	All DDR3 speed grades

Step 1: The BIOS first determines the common operating frequency of all modules in the system, ensuring that the corresponding value of tCK (tCKactual) falls between tCKmin (Byte 186/221) and tCKmax. If tCKactual is not a JEDEC standard value, the next smaller standard tCKmin value is used for calculating Write Recovery.

Step 2: The BIOS then calculates the “desired” Write Recovery (WRdesired):

WRdesired = ceiling (tWRmin / tCKactual)

where tWRmin is defined in Byte 17. The ceiling function requires that the quotient be rounded up always.

Step 3: The BIOS then determines the “actual” Write Recovery (WRactual):

WRactual = max (WRdesired, min WR supported)

where min WR is the lowest Write Recovery supported by the DDR3 SDRAM. Note that not all WR values supported by DDR3 SDRAMs are sequential, so the next higher supported WR value must be used in some cases.

Usage example for DDR3-1333G operating at DDR3-1333:

tCKactual = 1.5 ns
WRdesired = 15 / 1.5 = 10
WRactual = max(10, 10) = 10

Byte 194 or 229: Upper Nibbles for t_{RAS} and t_{RC}

This byte defines the most significant nibbles for the values of tRAS (byte 195/230) and tRC (byte 196/231). This value is based off but may exceed the DDR3 SDRAM data sheet.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
t_{RC} Most Significant Nibble	t_{RAS} Most Significant Nibble
See Byte 23 description	See Byte 22 description

Byte 195 or 230: Minimum Active to Precharge Delay Time (t_{RAS}min), Least Significant Byte

The lower nibble of Byte 194/229 and the contents of Byte 195/230 combined create a 12-bit value which defines the minimum SDRAM Active to Precharge Delay Time in medium timebase (MTB) units. The most significant bit is Bit 3 of Byte 194/229, and the least significant bit is Bit 0 of Byte 195/230. This value is based off but may exceed the DDR3 SDRAM data sheet.

Byte 194/229 Bit 3 ~ Bit 0, Byte 195/230 Bit 7 ~ Bit 0
Minimum Active to Precharge Time (t_{RAS}) MTB Units
Values defined from 1 to 4095

Examples:

tRAS (MTB units)	Timebase (ns)	tRAS Result (ns)	Use
300	0.125	37.5	DDR3-800D
300	0.125	37.5	DDR3-800E
300	0.125	37.5	DDR3-1066E
300	0.125	37.5	DDR3-1066F
300	0.125	37.5	DDR3-1066G
288	0.125	36	DDR3-1333F
288	0.125	36	DDR3-1333G
288	0.125	36	DDR3-1333H
288	0.125	36	DDR3-1333J
280	0.125	35	DDR3-1600G
280	0.125	35	DDR3-1600H
280	0.125	35	DDR3-1600J
280	0.125	35	DDR3-1600K

Byte 196 or 231: Minimum Active to Active/Refresh Delay Time (t_{RC}min), Least Significant Byte

The upper nibble of Byte 194/229 and the contents of Byte 196/231 combined create a 12-bit value which defines the minimum SDRAM Active to Active/Refresh Delay Time in medium timebase (MTB) units. The most significant bit is Bit 7 of Byte 194/229, and the least significant bit is Bit 0 of Byte 196/231. This value is based off but may exceed the DDR3 SDRAM data sheet.

Byte 194/229 Bit 7 ~ Bit 4, Byte 196/231 Bit 7 ~ Bit 0
Minimum Active to Active/Refresh Time (t_{RC}) MTB Units
Values defined from 1 to 4095

Examples:

tRC (MTB units)	**Timebase (ns)**	**tRC Result (ns)**	**Use**
400	0.125	50	DDR3-800D
420	0.125	52.5	DDR3-800E
390	0.125	48.75	DDR3-1066E
405	0.125	50.625	DDR3-1066F
420	0.125	52.5	DDR3-1066G
372	0.125	46.5	DDR3-1333F
384	0.125	48	DDR3-1333G
396	0.125	49.5	DDR3-1333H
408	0.125	51	DDR3-1333J
360	0.125	45	DDR3-1600G
370	0.125	46.25	DDR3-1600H
380	0.125	47.5	DDR3-1600J
390	0.125	48.75	DDR3-1600K

Byte 197 or 232: Maximum tREFI Time (Average Periodic Refresh Interval), Least Significant Byte

Byte 198 or 233: Maximum tREFI Time (Average Periodic Refresh Interval), Most Significant Byte

The contents of Bytes 197/232 and the contents of Bytes 198/233 combined create a 16-bit value which defines the maximum SDRAM tREFI Time in medium timebase (MTB) units. The most significant bit is Bit 7 of Byte 198/233, and the least significant bit is Bit 0 of Byte 197/232. This value is based off but may exceed the DDR3 SDRAM data sheet. NOTE: Timebase in uS not nS.

Byte 198/233 Bit 7 ~ Bit 0, Byte 197/232 Bit 7 ~ Bit 0
Maximum tREFI Time (tREFImax) MTB Units
Values defined from 1 to 65535

Examples:

tREFI (MTB units)	Timebase (us)	tREFI Result (us)	Use
31	0.125	~3.9	Typical 2X Refresh rate
63	0.125	~7.8	Standard 1X Refresh Rate
125	0.125	~15.6	1/2 Standard Refresh Rate - 2x Performance
250	0.125	~31.2	1/4 Standard Refresh Rate - 4x Performance
499	0.125	~62.4	1/8 Standard Refresh Rate - 8x Performance

Byte 199 or 234: Minimum Refresh Recovery Delay Time (t_{RFC}min), Least Significant Byte
Byte 200 or 235: Minimum Refresh Recovery Delay Time (t_{RFC}min), Most Significant Byte

The contents of Bytes 199/234 and the contents of Bytes 200/235 are combined to create a 16-bit value which defines the minimum SDRAM Refresh Recovery Time Delay in medium timebase (MTB) units. The most significant bit is Bit 7 of Byte 200/235, and the least significant bit is Bit 0 of Byte 199/234. This value is based off but may exceed the DDR3 SDRAM data sheet.

Byte 200/235 Bit 7 ~ Bit 0, Byte 199/234 Bit 7 ~ Bit 0
Minimum Refresh Recover Time Delay (t_{RFC}) MTB Units
Values defined from 1 to 65535

Examples:

tRFC (MTB units)	Timebase (ns)	tRFC Result (ns)	Use
720	0.125	90	512 Mb
880	0.125	110	1 Gb
1280	0.125	160	2 Gb

Byte 201 or 236: Minimum Internal Read to Precharge Command Delay Time (t_{RTP}min)

This byte defines the minimum SDRAM Internal Read to Precharge Delay Time in medium timebase (MTB) units. This value comes from the DDR3 SDRAM data sheet. The value of this number may be dependent on the SDRAM page size; please refer to the DDR3 SDRAM data sheet section on Addressing to determine the page size for these devices. Controller designers must also note that at some frequencies, a minimum number of clocks may be required resulting in a larger tRTPmin value than indicated in the SPD. Note: DDR3 supports a min t_{RTP} of 4tCK by design, there will be no benefit from trying to go below this value.

Bit 7 ~ Bit 0
Internal Read to Precharge Delay Time (t_{RTP}) MTB Units
Values defined from 1 to 255

Examples:

tRTP (MTB units)	Timebase (ns)	tRTP Result (ns)	Use
60	0.125	7.5	All DDR3 SDRAM speed bins

Byte 202 or 237: Minimum Row Active to Row Active Delay Time (t_{RRD}min)

This byte defines the minimum SDRAM Row Active to Row Active Delay Time in medium timebase units. This value is based off but may exceed the DDR3 SDRAM data sheet. The value of this number may be dependent on the SDRAM page size; please refer to the DDR3 SDRAM data sheet section on Addressing to determine the page size for these devices. Controller designers must also note that at some frequencies, a minimum number of clocks may be required resulting in a larger tRRDmin value than indicated in the SPD. Note: DDR3 supports a min t_{RRD} of 4tCK by design, there will be no benefit from trying to go below this value.

Bit 7 ~ Bit 0
Minimum Row Active to Row Active Delay (t_{RRD}) MTB Units
Values defined from 1 to 255

Examples:

tRRD (MTB units)	Timebase (ns)	tRRD Result (ns)	Use
48	0.125	6.0	Example: DDR3-1333, 1KB page size
60	0.125	7.5	Example: DDR3-1333, 2KB page size
80	0.125	10	Example: DDR3-800, 1KB page size

Byte 203 or 238: Upper Nibble for t_{FAW}

This byte defines the most significant nibble for the value of tFAW (SPD byte 204/239). This value comes from the DDR3 SDRAM data sheet.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
Reserved	t_{FAW} Most Significant Nibble
Reserved	See Byte 29 description

Byte 204 or 239: Minimum Four Activate Window Delay Time (t_{FAW}min), Least Significant Byte

The lower nibble of Byte 203/238 and the contents of Byte 204/239 combined create a 12-bit value which defines the minimum SDRAM Four Activate Window Delay Time in medium timebase (MTB) units. This value comes from the DDR3 SDRAM data sheet. The value of this number may be dependent on the SDRAM page size; please refer to the DDR3 SDRAM data sheet section on Addressing to determine the page size for these devices.

Byte 203/238 Bit 3 ~ Bit 0, Byte 204/239 Bit 7 ~ Bit 0
Minimum Four Activate Window Delay Time (t_{FAW}) MTB Units
Values defined from 1 to 4095

Examples:

tFAW (MTB units)	Timebase (ns)	tFAW Result (ns)	Use
320	0.125	40.0	Example: DDR3-800, 1 KB page size
400	0.125	50.0	Example: DDR3-800, 2 KB page size
300	0.125	37.5	Example: DDR3-1066, 1 KB page size
400	0.125	50.0	Example: DDR3-1066, 2 KB page size
240	0.125	30.0	Example: DDR3-1333, 1 KB page size
360	0.125	45.0	Example: DDR3-1333, 2 KB page size
240	0.125	30.0	Example: DDR3-1600, 1 KB page size
320	0.125	40.0	Example: DDR3-1600, 2 KB page size

Byte 205 or 240: Minimum Internal Write to Read Command Delay Time (t_{WTR}min)

This byte defines the minimum SDRAM Internal Write to Read Delay Time in medium timebase (MTB) units. This value comes from the DDR3 SDRAM data sheet. The value of this number may be dependent on the SDRAM page size; please refer to the DDR3 SDRAM data sheet section on Addressing to determine the page size for these devices. Controller designers must also note that at some frequencies, a minimum number of clocks may be required resulting in a larger tWTRmin value than indicated in the SPD. Note: DDR3 supports a min t_{WTR} of 4tCK by design, there will be no benefit from trying to go below this value

Bit 7 ~ Bit 0
Internal Write to Read Delay Time (t_{WTR}) MTB Units
Values defined from 1 to 255

Examples:

tWTR (MTB units)	Timebase (ns)	tWTR Result (ns)	Use
60	0.125	7.5	All DDR3 SDRAM speed bins

Byte 206 or 241: Write to Read & Read to Write CMD Turn-around Time Optimizations

This byte describes the ability to 'potentially' remove some of the turn around time spacing between read and write commands. These turn around times have multiple dependence which may cause it to fail.

Important Note: This byte does not use MTB.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
Read to Write CMD Turn-around Time	Write to Read CMD Turn-around Time
Bit [7, 6, 5, 4] : 0000 = Default - No adjustment 0001 = 1 Clock Pull-in 0010 = 2 Clock Pull-in 0011 = 3 Clock Pull-in 0100 = 4 Clock Pull-in 0101 = 5 Clock Pull-in 0110 = 6 Clock Pull-in 0111 = 7 Clock Pull-in 1000 = RSVD 1001 = 1 Clock Push-out 1010 = 2 Clock Push-out 1011 = 3 Clock Push-out 1100 = 4 Clock Push-out 1101 = 5 Clock Push-out 1110 = 6 Clock Push-out 1111 = 7 Clock Push-out	Bit [3, 2, 1, 0] : 0000 = Default - No adjustment 0001 = 1 Clock Pull-in 0010 = 2 Clock Pull-in 0011 = 3 Clock Pull-in 0100 = 4 Clock Pull-in 0101 = 5 Clock Pull-in 0110 = 6 Clock Pull-in 0111 = 7 Clock Pull-in 1000 = RSVD 1001 = 1 Clock Push-out 1010 = 2 Clock Push-out 1011 = 3 Clock Push-out 1100 = 4 Clock Push-out 1101 = 5 Clock Push-out 1110 = 6 Clock Push-out 1111 = 7 Clock Push-out

Byte 207 or 242: Back 2 Back CMD Turn-around Time Optimizations

Turn around times have multiple system and SDRAM dependence which may cause it to fail. There is a JEDEC specification for the min turn around time between commands (tCCD) but in normal system usage, platform limitations/considerations sometimes increase that above the burst size. This byte describes the ability to 'potentially' remove some of the turn around time spacing between commands.

Important Note: This byte does not use MTB.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
Reserved	Back to Back CMD Turn-around Time
Reserved	Bit [3, 2, 1, 0] : 0000 = Default - No adjustment 0001 = 1 Clock Pull-in 0010 = 2 Clock Pull-in 0011 = 3 Clock Pull-in 0100 = 4 Clock Pull-in 0101 = 5 Clock Pull-in 0110 = 6 Clock Pull-in 0111 = 7 Clock Pull-in 1000 = RSVD 1001 = 1 Clock Push-out 1010 = 2 Clock Push-out 1011 = 3 Clock Push-out 1100 = 4 Clock Push-out 1101 = 5 Clock Push-out 1110 = 6 Clock Push-out 1111 = 7 Clock Push-out

Byte 208 or 243: System CMD Rate Mode

This byte defines the command rate used on the Address, Command and Control Bus. This value typically ranges from 1n to 3n (1n being the highest performance but requires a robust dataeye which may be impossible with some loading configurations and frequencies).

Important Note: This byte redefines MTB to tCK instead of ns.

Bit 7 ~ Bit 0
System CMD Rate Mode MTB Units
0 - Not Defined - System Operates in default command mode Other settings defined from 1 to 254

Example:

CMD Rate (MTB units)	Timebase (tCK)	CMD Rate Result (tCK)	Use
0	0.125	0	System Operates in Default mode
8	0.125	1	System Operates in 1n Command Rate Mode
16	0.125	2	System Operates in 2n Command Rate Mode
24	0.125	3	System Operates in 3n Command Rate Mode

Note: Not all modes shown in example may be used. Additionally, other modes not shown are not currently supported.

Byte 209 or 244: SDRAM Auto Self Refresh Performance (Sub 1x Refresh and IDD6 impact)

This byte describes the module's ability to support Auto Self Refresh in sub 1x modes.
Clarification of byte use TBD

Bytes 210-218: Reserved for Profile 1 Section

Bytes 245-253: Reserved Profile 2 Section

Byte 219 or 254: Vendor Personality Byte - RSVD

This byte is reserved for vendor specific personality bits. This specification will not define the contents of this byte but will simply reserve it for vendor specific use. Each profile will have it's own personality byte.

Bit 7 ~ Bit 0
Vendor Personality Bits

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