
Mobile DRAM's Frequently violated parameters Application Note

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Purpose

Using SDR or DDR mobile DRAM, based on our survey, most frequently violated points are tRFC, tRAS, tDS, tXSR and CAS latency related. In this application note, these items will be explained in detail: the meaning of these parameters, and how to measure and find out the violated point from your system. This will be helpful for mobile system software and hardware engineers.

References

- Samsung SDR Mobile DRAM Databook (Specification Book)
- Samsung DDR Mobile DRAM Databook (Specification Book)



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1. tRFC Violation

1.1 Definition and explanation

tRFC (Auto refresh cycle time) is a minimum delay time from an auto-refresh to any next command. This delay is needed to finish an auto-refresh. See the below (Figure1) timing. For example, if tRFC is minimum 80ns and your system's clock frequency is 100MHz, the time gap from auto-refresh to next command should be at least 8 clocks.

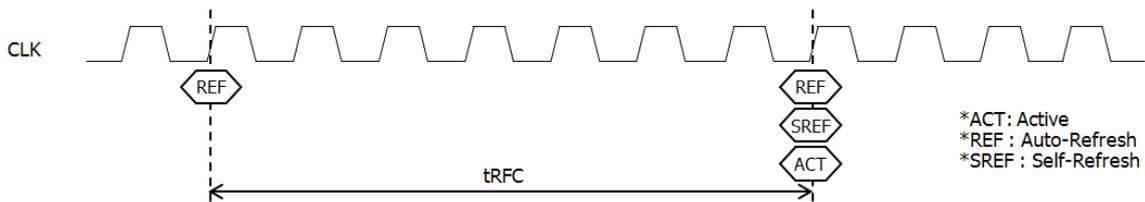


Figure1. Timing: tRFC

1.2 Violation case review

- Failure phenomenon: System reset or hang-up during/ after booting
 - tRFC value: minimum 80ns @ K5E1H12ACM (NAND 1Gb + mDDR 512Mb)
- (This value might vary with each SDR/DDR device, please refer to the Databook.)

See the logic analyzer timing of tRFC violation below, Figure2.

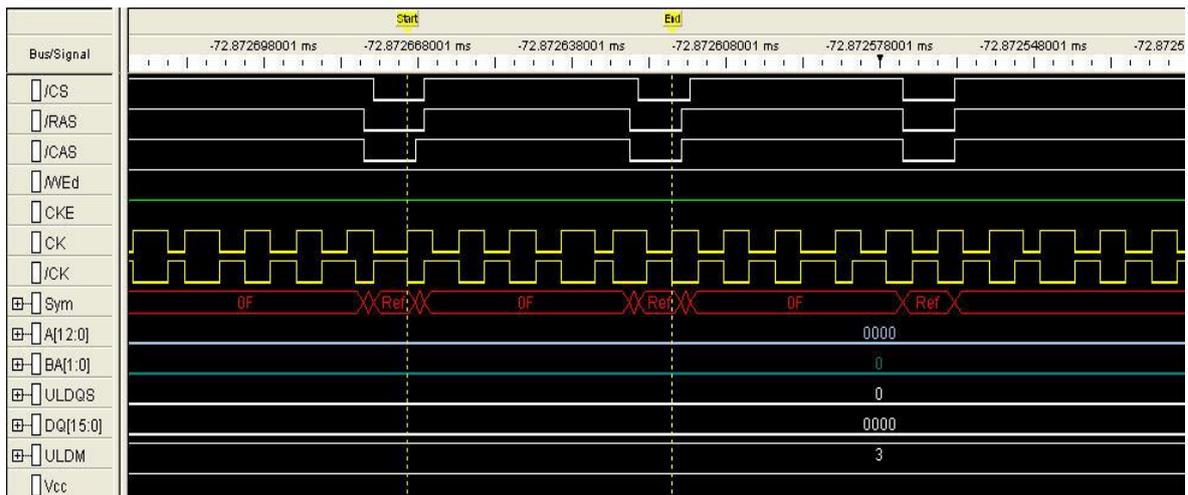


Figure2. Timing: tRFC violation

Failure description

The time between two refreshes (where the cursors located) is 52ns, which is smaller

than the specification value. In this case, the second refresh opens a row before the first refresh closes a previous row. This makes a collision of two rows, causing data corruption.

In this case, system's idle mode uses both low and high frequencies in turn. For high frequency (96MHz, 10.4ns period), tRFC is 10 clocks which is 104ns. For low frequency (9.6MHz, 104ns period), tRFC is 5 clocks which is 520ns. However when frequency changes from low to high, the clock-based-setting changes little later than frequency changes. (It's a chipset's bug.) Intermittently, burst refresh commands are issued at this moment, for high frequency (96MHz, 10.4ns); tRFC becomes 5 clocks which is only 52ns.

Solution

Though the root cause is from chipset's bug, it might be temporarily solved by either uniformly issuing refresh command (not using burst refresh) or setting tRFC always 10 clocks no matter what frequency is.

1.3 How to measure

To check tRFC value on your system, you need to probe at least four signals: /CS, /RAS, /CAS, /WE. If you use logic analyzer, go to trigger functions, choose 'Edge followed by edge' or 'Edge followed by pattern'. Setup the condition like the below, figure3.

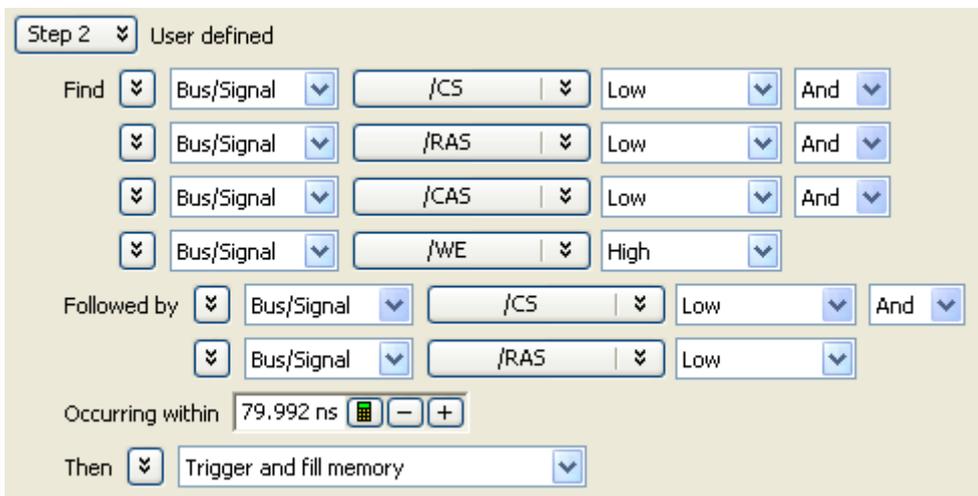


Figure3. Trigger condition for tRFC

Figure3 means that if any command is followed by refresh command within 80ns, then trigger. Unless your system has a violation related to tRFC, it will not be triggered for whole operation of your system.



1.4 Failure tendency

Failure related to tRFC might occur more frequently in hot temperature and low Vdd than in cold temperature and high Vdd. It has no relationship with clock speed or memory's driver strength.

2. tRAS Violation

2.1 Definition and explanation

tRAS (Row active time) is from active command to the same bank or all bank precharge command. See the below (Figure4) timing. For example, if tRAS is minimum 45ns / maximum 70us and your system's clock frequency is 100MHz, the time gap from active to its precharge should be between 5 clocks and 7,000 clocks.

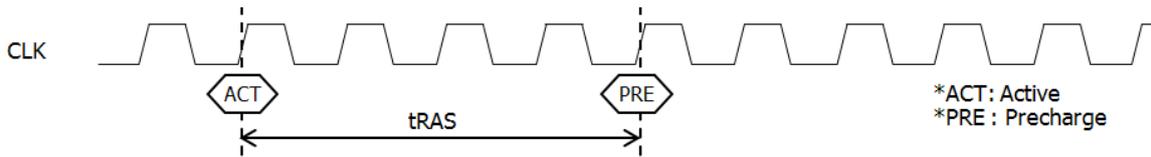


Figure4. Timing: tRAS

2.2 Violation case review

- Failure phenomenon: System reset or hang-up during wake-up or stand-by
 - tRAS value: min 45ns / max 70us @ K5E1H12ACM (NAND 1Gb + mDDR 512Mb)
- (This value might vary with each SDR/DDR device, please refer to the Databook.)

See the logic analyzer timing of tRFC violation below, Figure5.

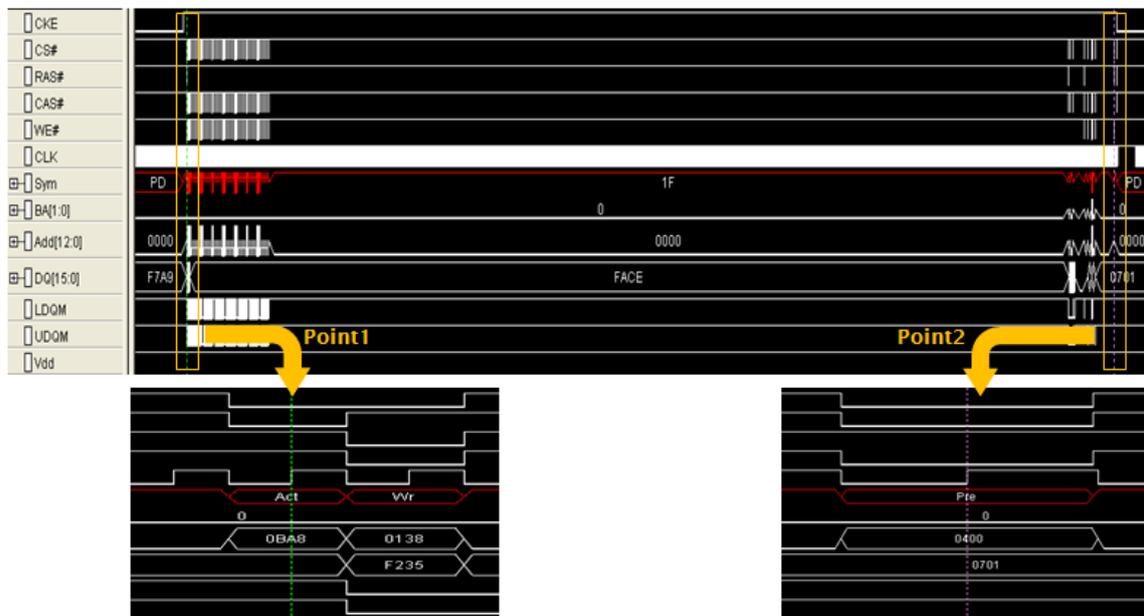


Figure5. Timing: tRAS max violation

Failure description

The time between active (point1) to precharge (point2) is 281us. Since tRAS maximum

is 70us, it is out of specification. In this case, there is no register for tRAS max in chipset's code. (Normally, chipset has a register to control tRAS max.)

tRAS is a delay time to restore the sensing data after active command. If it is too short, data might not be fully restored, so its cell data might be uncertain. On the other hand, if it is too long, this means that a row is opened for that long time without performing refresh, the weakest bit might leak its data.

2.3 How to measure

To check minimum value of tRAS value on your system, you need to probe at least seven signals: /CS, /RAS, /CAS, /WE, BA[1:0], Add[10]. If using logic analyzer, go to trigger functions, choose 'Edge followed by pattern'. Setup the condition like the below, figure6.

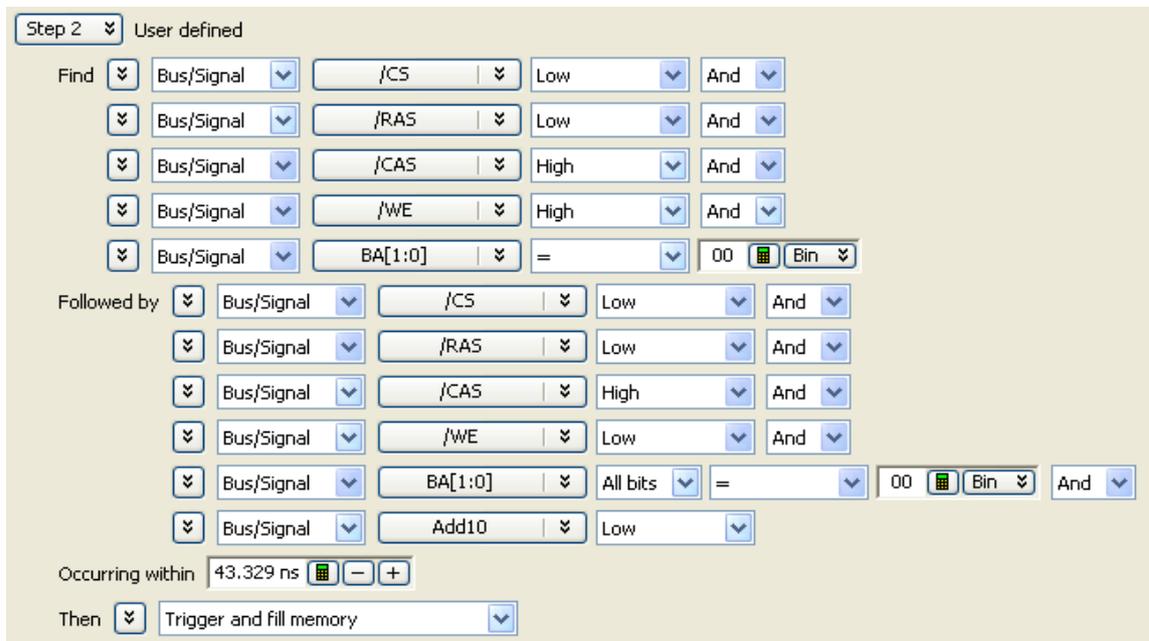


Figure6. Trigger condition for tRAS minimum

Figure6 means that if active command is followed by its precharge command within 45ns, then trigger. For searching in case of all bank precharge, change BA[1:0] = XX (Don't care) and Add10 = high. Unless your system has a violation related to tRAS, it will not be triggered for whole operation of your system.

For checking maximum value of tRAS, choose 'Pattern too late after edge'. Setup the condition like the below, figure7.

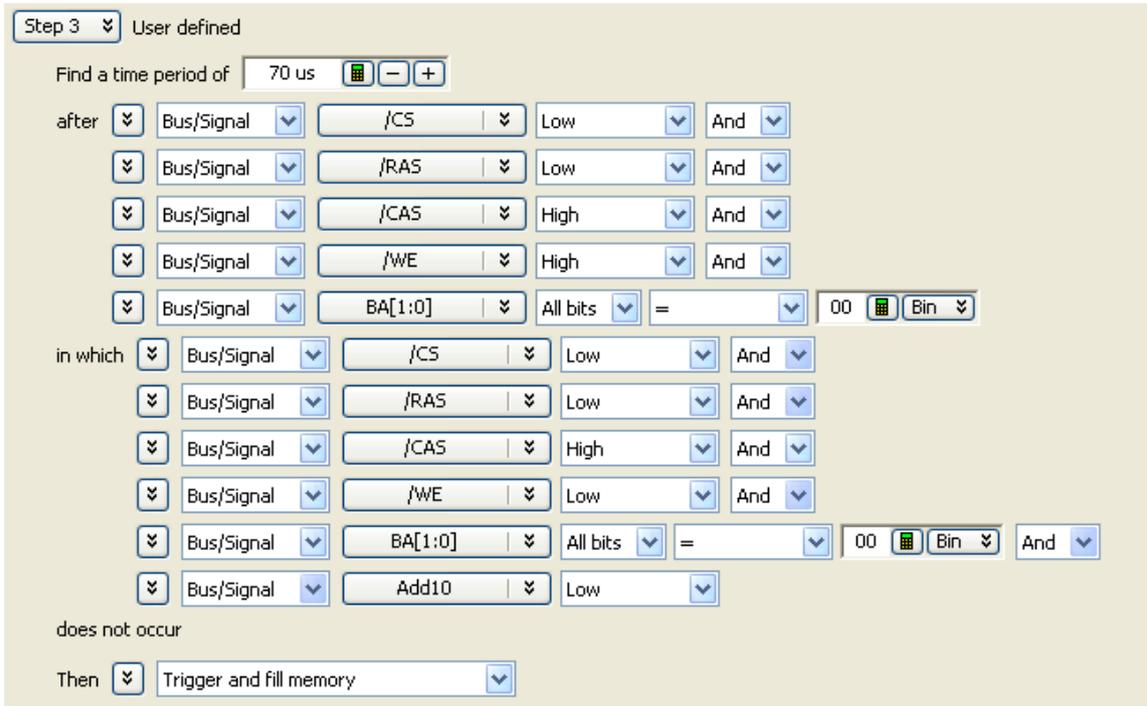


Figure7. Trigger condition for tRAS maximum

Figure7 means that if active command is not followed by its precharge command within 70us, then trigger. For searching in case of all bank precharge, change BA[1:0] = XX (Don't care) and Add10 = high. Unless your system has a violation related to tRAS, it will not be triggered for whole operation of your system.

2.4 Failure tendency

Failure related to tRAS might occur more frequently in hot temperature and low Vdd than in cold temperature and high Vdd. It has no relationship with clock speed or memory's driver strength.

3. tDS Violation

3.1 Definition and explanation

tDS is DQs and DMs' setup time to DQS. See the below (Figure8) timing. For example, if tDS minimum is 600ps, the time gap from starting of valid data to DQS rising should be at least 600ps. This is only for write operation, not for read operation. DQS0/DM0 should be matched with DQ0 thru DQ7, DQS1/DM1 with DQ8 thru DQ15, DQS2/DM2 with DQ16 thru DQ23, DQS3/DM3 with DQ24 thru DQ31, respectively.

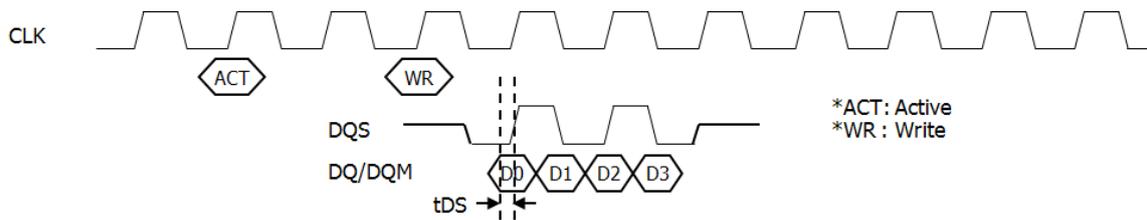


Figure8. Timing: tDS

3.2 Violation case review

- Failure phenomenon: On DRAM test PGM, checksum failed.
 - tDS value: min 800ps @ K4X12163PC (mDDR 512Mb)
- (This value might vary with each SDR/DDR device, please refer to the Databook.)

See the scope screen of tDS violation below, Figure9.

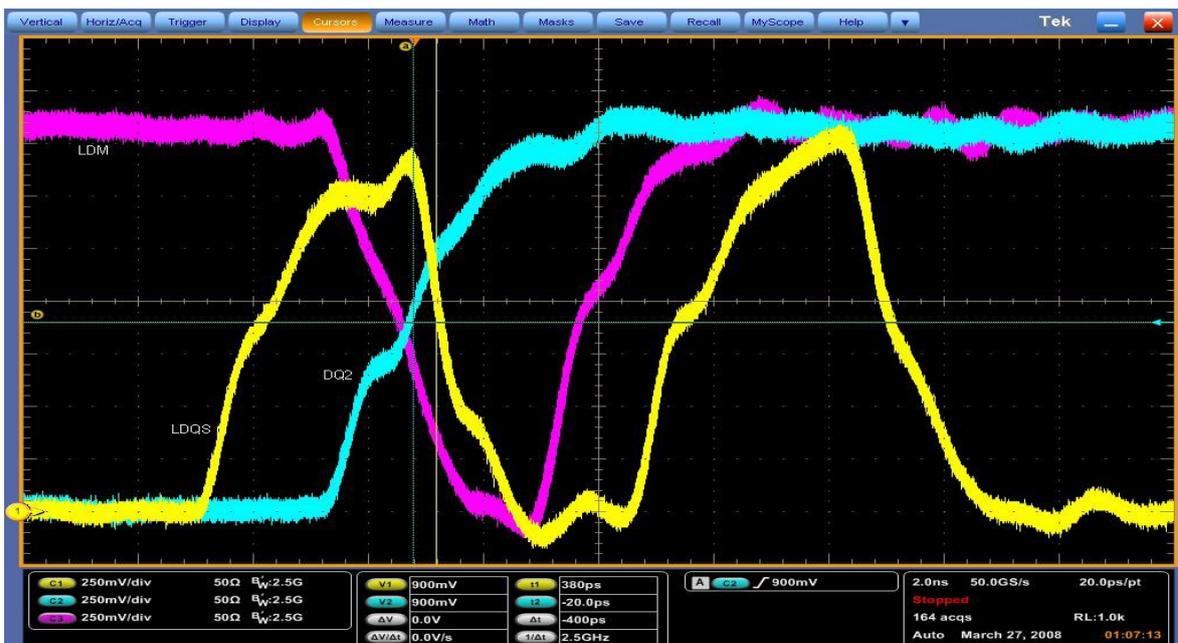


Figure9. Scope shot: tDS violation

Failure description

In figure9, DDR's write timing, time gap from DQ's rising edge to LDQS's first falling edge is only 400ps which is not enough time (min 800ps) to perform write operation.

3.3 How to measure

To check tDS value on your system, you need to probe at least two signals: DQS, DQ or DQS, DM. Recommended oscilloscope's bandwidth is 10 times of clock frequency. For example, if clock is 100MHz, it is recommended to use at least 1GHz bandwidth oscilloscope not to distort the signal wave. To measure tDS, check the time gap from half point of DQ's rising or falling to half point of DQS rising or falling. With the same way, you can check DM's setup time instead of DQs. In case of SDR, measure CLK signal instead of DQS.

3.4 Failure tendency

Failure related to tDS might occur more frequently in hot temperature, high frequency and low Vdd than in cold temperature, low frequency and high Vdd. Generally, the bigger the driver strength of chipset, the better tDS margin due to enhanced rising/falling time and the worse noise immunity due to the ring back noise.

Failure description

In figure11, clock speed is 71MHz, and CAS latency is 2. CL is set as 2, phone developer tests with clock speed changing, 90MHz/71MHz/61Mhz/19.2MHz/9.6MHz. Failure occurs only when 90MHz/71MHz, which is out of specification. If frequency is 90MHz or 71 MHz, CL value should be 3, 2 will be not enough long.

4.3 How to measure

To check CAS latency of your system, you need to check MRS code by software.

	DDR266	DDR333	DDR400
Speed @CL2 ¹⁾	83Mhz	83Mhz	83Mhz
Speed @CL3 ¹⁾	133Mhz	166Mhz	200Mhz

Figure12. CAS latency with clock freq.

Figure12 shows possible clock speeds according to CAS latency value, 2 or 3. For example, if using DDR333 and MRS sets CAS latency 2, DRAM's clock speed should be no more than 83MHz.

4.4 Failure tendency

Failure related to CAS latency might occur more frequently in hot temperature, high frequency and low Vdd than in cold temperature, low frequency and high Vdd. It has no relationship with memory's driver strength.

5. tXSR Violation

5.1 Definition and explanation

tXSR is delay time from self-refresh exit command to next command. See the below (Figure13) timing. For example, if tXSR minimum is 120ns and your system's speed is 100MHz (10ns period), the time gap from self-refresh exit to next valid command should be at least 12 clocks.

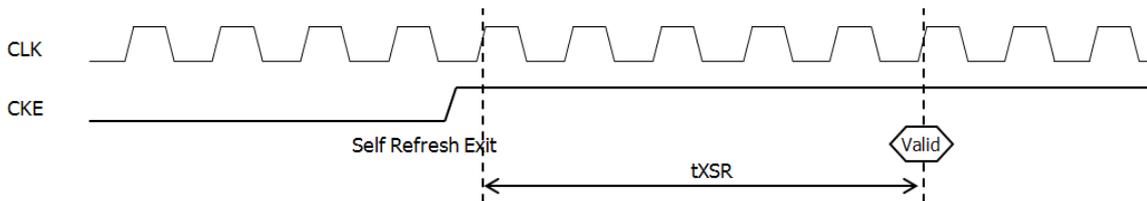


Figure13. Timing: tXSR

5.2 Violation case review

- Failure phenomenon: Lock up or reset during sleep mode or wake-up
- tXSR value: min 120ns @ K5E1H12ACM (NAND 1Gb + mDDR 512Mb)
(This value might vary with each SDR/DDR device, please refer to the Databook.)

See the logic analyzer timing of tXSR violation below, Figure14.

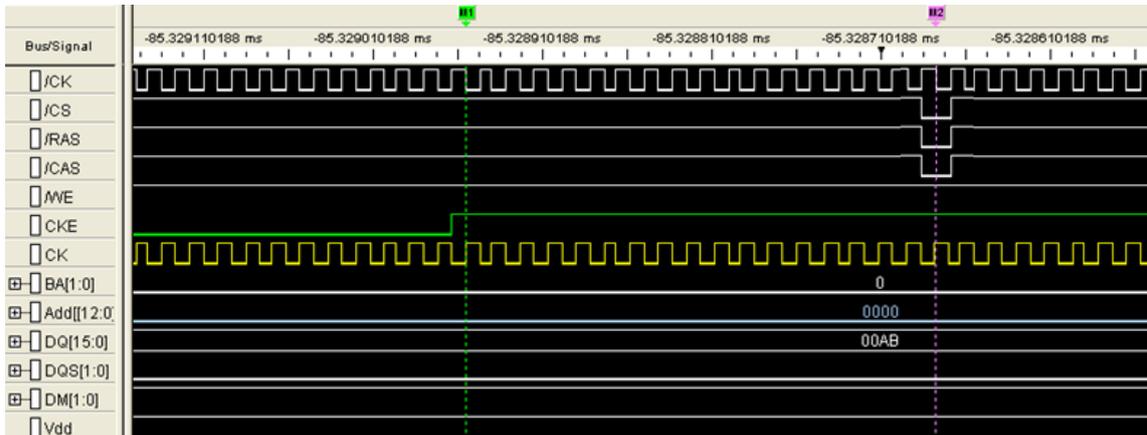


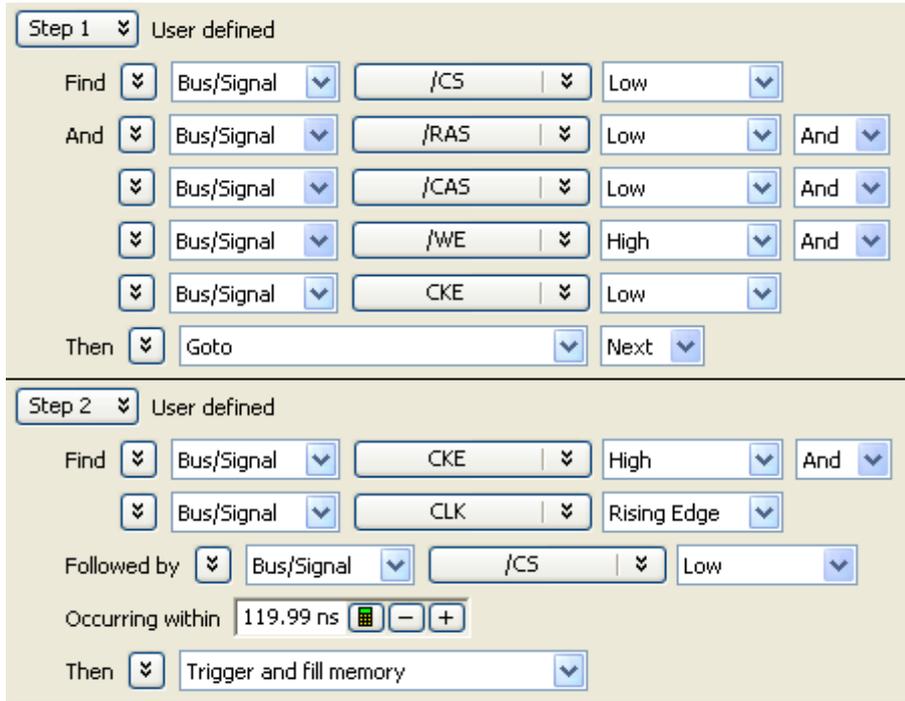
Figure14. Timing: tXSR violation

Failure description

In figure14, the time gap from self-refresh exit to refresh command is only 110ns, which is out of specification. In this case, tXSR value is 17 clocks. To avoid potential failure, it should be at least 19 clocks or above.

5.3 How to measure

To check tXSR value on your system, you need to probe at least three signals: CKE, CLK, /CS. If using logic analyzer, go to trigger functions, choose 'Edge followed by pattern'. Setup the condition like the below, figure15.



The screenshot shows a logic analyzer trigger configuration window with two steps:

- Step 1:** User defined. Find Bus/Signal /CS Low. And Bus/Signal /RAS Low. And Bus/Signal /CAS Low. And Bus/Signal /WE High. And Bus/Signal CKE Low. Then Goto Next.
- Step 2:** User defined. Find Bus/Signal CKE High. And Bus/Signal CLK Rising Edge. Followed by Bus/Signal /CS Low. Occurring within 119.99 ns. Then Trigger and fill memory.

Figure15. Trigger condition for tXSR minimum

Figure15 means that, step1 is for entering self-refresh mode, and then step2, if self-refresh exit command is followed by any command within 120ns, then trigger. System usually uses self-refresh mode (repeatedly enter and exit) when it is in sleep/ idle mode. Unless your system has a violation related to tXSR, it will not be triggered for whole operation of your system.

5.4 Failure tendency

Failure related to tXSR might occur more frequently in hot temperature than in cold temperature. It has no relationship with clock speed, Vdd or memory's driver strength.